

VIDEOLOGY

IMAGING SOLUTIONS INC.
Original Equipment Manufacturer

Application Note

20/21D386 (Board Mount)

20/21D389 (CS Mount)

High Resolution

Monochrome Camera Modules
Including FS fast shutter speed models

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1. Introduction:

The 20/21D389 is a B/W high-resolution camera module designed around the Sony Exview® high resolution 1/3 "CCD sensor.

The camera offers multiple features including digital video output, external Horizontal and Vertical Synchronization, asynchronous reset, an external control of shutter speed, gain, gamma etc. via a serial I2C type communication port. A programmable on board CPLD can also be used to provide additional functionality.

The 20D389FS model also offers high speed (field by field) control of both the shutter speed and gain, making this camera ideal for applications involving fast moving objects under varying lighting conditions (car license plate capture for example).

The camera offers good near infra red (IR) sensitivity, making it ideal for use with IR illumination systems.

The camera is a single board design measuring 42 mm square, and is available with a CS or board lens mount.

2. Revisions History

Revision	Issue Date	Details	CN#
A	4/01/2003	Software - Hardware change Added Field / Frame Integration Added digital output format Changed Synchronization modes Removed Sync. Lock	N/A
B	1202/3120/20032004 01-30-2004	Added digital output format	04-0127
C	05/24/2004	Updated board drawings – Section 6. 1	04-0213
D	08/25/2005	Software Control 5.1 update	05-0599
E	02/07/2007	Section 4.1 Fixed Shutter Speed	07-0027
F	07/09/2007	Section 4.1 Fixed Shutter Speed	07-0146
G	05/07/10	Added Fast Shutter Speed Control	10-0086

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3. Camera Features

features:

B&W camera, which is controllable via I²C
CCD 768/752 pixels, (horizontal) resolution >560 TVL
Integrated Auto Exposure Control (Iris/AGC)
Edge enhancement
Gamma (0.45) or (1), Default (0.45)
Sensitivity 30 IRE lens F1.2: 0.001 Lux

Additional features of the 20/21D389 main board are:

Synchronization modes:
Internal X-tal locked
External H and V
External line lock
External sync-lock
A-synchronous reset
Fixed shutter speeds (8 values including flicker-less)
Manual gain control (via I²C control software)
Back light compensation on/off (default on)
Supply voltage +12V DC (+ 3V / - 4V)
Mirror mode
8-bit Digital Output

Additional features of the 20/21D389FS models:

High-speed field-by-field control of shutter speed from 1/200s to 1/100,000 s.
High-speed field-by-field control of gain.

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4. Camera Module Functionality

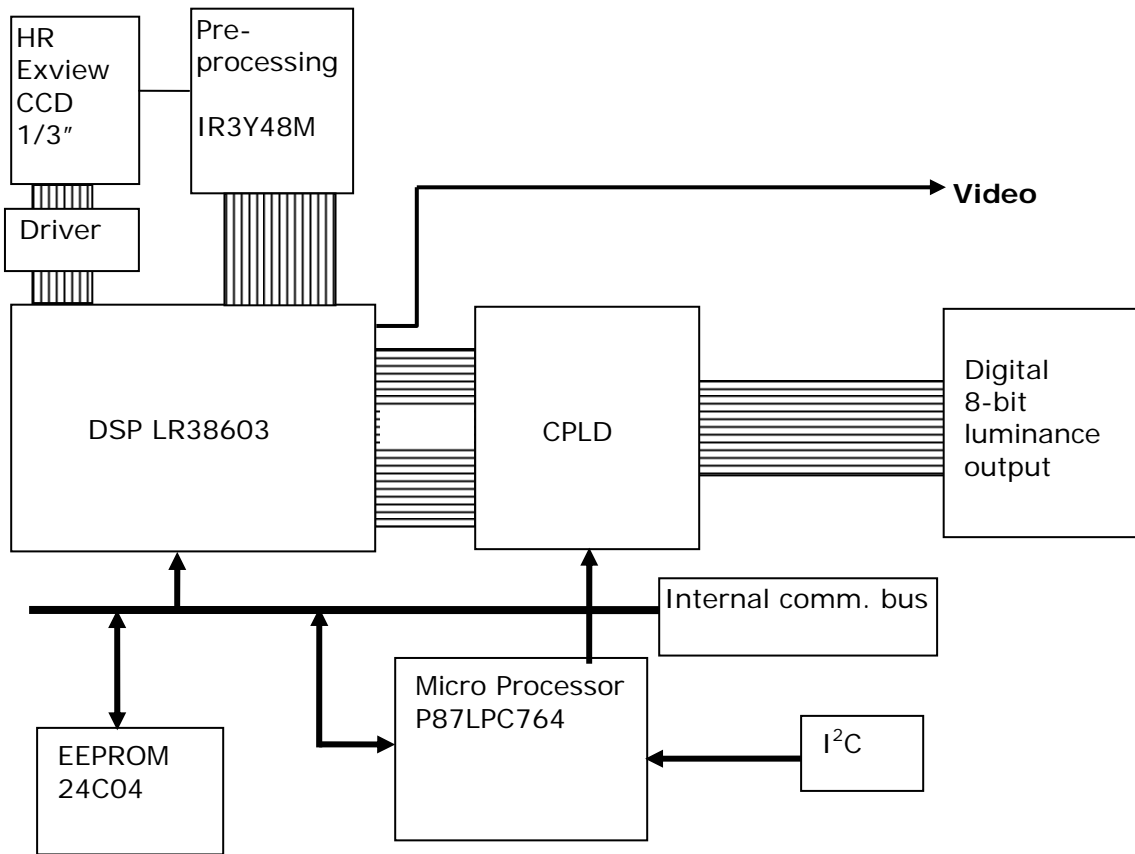


Figure 1. Block diagram

The CPLD is re-programmable for extra functionality. Some extra coding or featuring can also be done, but only on the digital output.

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The following functions are possible with the 20/21D389 camera-module:

5. Shutter Speed Control

In default mode, the camera operates in the electronic iris mode. This means the output of the CCD, which is dependent on the light intensity, is controlled by the electronics of the camera and not the mechanics of the lens. To do this the camera has an OFD pulse. When this OFD pulse is active (Low see Figure 2) the charge that is built up in the photo diodes is dumped into the substrate of the CCD. So after each OFD pulse the accumulation of the charge in the photocells of the CCD start from zero. The amount of signal out of the CCD is dependent on the light intensity and the time that the charge can build up (the period during which no OFD pulse is present). Therefore, by measuring the output of the CCD and comparing it with an internal reference it is possible to control the level of the signal out of the CCD (within a certain tolerance).

However, sometimes it is preferred that the shutter is fixed and not automatic. An example where using a fixed shutter is beneficial is if there is a very fast moving object in the scene. The longer the integration time (the period that no OFD pulse occurs, max 1/50 sec for CCIR and max 1/60 sec for EIA) the less sharp the image will be due to movement of the object during the integration period. To prevent this the camera has 8 fixed shutter speeds (see table 1). To switch the electronic iris off there are two options: Either via I²C software control or via hardware control. In the last mode it is required that the module gets a special software setting (command setting 06h should be loaded with FFh to force the camera in hardware control).

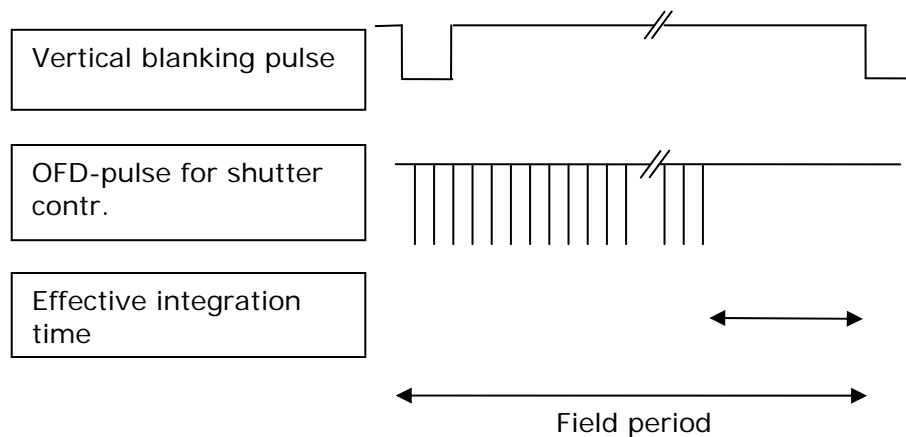


Figure 2. Shutter Control

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Shutter Speed		Command address 06h	PROG-MODE 1	PROG-MODE 2	PROG-MODE 3	PROG-MODE 4
20D389 (EIA)	21D389(CCIR)					
1/60 sec (max)	1/50 (max)	0xff	high	low	low	low
1/100 sec (flickerless)*	1/120 sec (flickerless)*	0xff	high	low	low	high
1/250 second		0xff	high	low	high	Low
1/500 second		0xff	high	low	high	high
1/1000 second		0xff	high	high	low	Low
1/2000 second		0xff	high	high	low	high
1/10000 second		0xff	high	high	high	Low
1/20000 second		0xff	high	high	high	high
Auto mode		0x00	x	x	x	x
1/60 sec (max)	1/50 (max)	0x01	x	x	x	x
1/100 sec (flickerless)*	1/120 sec (flickerless)*	0x02	x	x	x	x
1/250 second		0x03	x	x	x	x
1/500 second		0x04	x	x	x	x
1/1000 second		0x05	x	x	x	x
1/5000 2000 second		0x06	x	x	x	x
1/10000 second		0x07	x	x	x	x
1/20000 second		0x08	x	x	x	x
1/50000		0x09	x	x	x	x
1/100000		0x0a	x	x	x	x
1/30 second	1/25 second	0x0b	x	x	x	x
1/15 second	1/12.5 second	0x0c	x	x	x	x
1/7.5 second	1/6.25 second	0x0d	x	x	x	x

Table 1. Fixed Shutter Speed

Flickerless for the purpose of this document, is meant that a CCIR camera can be used in a 60 Hz (or a EIA camera in a 50 Hz) light environment without flickering due to fluorescent lighting.

In table 1 "low" stands for: connect connector pin to ground and "high" for connector pin open or connected to +3.3V.

PROG-MODE1, PROG-MODE2, PROG-MODE3 and PROG-MODE4 (PROGRAM-MODES) are on connector J710 but can also be fixed too low level (default high level) on camera board by populating resistor (shape 0402) R621 for PM1, resistor R625 for PM2, resistor R627 for PM3 and resistor R632 for PM4. Resistor mounted is equal to "low". Resistor not mounted is equal "high". Value resistor $\leq 1k\Omega$.

The default factory setting is that command register is loaded with 0x00 and all connector pins are High (open).

The lower three lines in the table are special modes. When using the extended integration times (1/30, 1/15 or 1/7.5 second) you will have to consider that these integration times will exceed normal video timing. This means that this will result in blinking video due to the missing fields. This mode is used to increase sensitivity of the camera even more. To get full advantage of these modes you need to use video-memory (to get continuous video) or use a capture board.

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5.1. High Speed Shutter Control Mode

There are applications in which it is very useful to be able to adjust both the camera shutter speed and gain very rapidly. A typical such application is car number plate capture. Because the car may be moving very rapidly, through what is a relatively small field of view, it is essential that the camera be able to make rapid changes to the shutter speed in order to cope with varying levels of illumination, number plate reflectivity, shadows etc.

Under normal operation, the shutter speed is controlled by the OFD pulses originating from the DSP. Changes to the DSP settings do not take effect until the field following the communications, and are not reflected in the output image until the field following that. Thus there is a delay of at least two fields before the new shutter speed settings are seen in the output of the camera, and by this time the car may be gone from the field of view.

To overcome this problem, the camera utilizes a novel method of controlling the shutter speed within the CPLD.

By using this approach, it is possible to change the shutter speed within the current field, provided that the command is sent within certain time limits.

5.1.1. Command Structure

The camera can be set to either auto shutter mode, or high speed shutter mode via the following command:

```
0x70 0x30 0xXX <data>
```

If data = 0 the camera will be put back in a normal mode (AGC and electronic iris). When data is not equal to zero the camera will be put in special high-speed control mode.

There are three command options for controlling the shutter speed and gain. Each command consists of 4 bytes. The functionality of each command type is described below.

5.2. Command One

Command type one provides for a selection of 8 fixed shutter speeds and variable gain. The data format is:

```
0x70 0x10 <shutter Speed> <gain data>
```

The available shutter speed values are listed in Table 1

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Table 2. Shutter speed settings (Command 1)

Shutter operand	Shutter speed	Gain Operand	Gain setting
0xc0	No change to the shutter value	0x00	No Change
0xd0	1/500 s	0x01-0xfe	New Gain setting
0xd 1	1/1000 s		
0xd 2	1/2000 s		
0xd 3	1/5000 s		
0xd 4	1/10000 s		
0xd 5	1/20000 s		
0xd 6	1/50000 s		
0xd 7	1/100000 s		

5.3. Command Two

Command type Two provides for a greater selection of shutter speeds than command one. Also in this mode, the shutter speed is always overwritten whereas in command type 1, it is possible to change only the gain and leave the shutter speed as is.

The data structure for command two is:

0x70 0x20 <shutter Speed> <gain data>

The shutter speed settings provided by the Command Two option are listed in Figure 3

Table 3. Shutter Speed Options for command type 2

Operand	Shutter speed	Operand	Shutter speed	Operand	Shutter speed
		1e	1/455	3e	1/2712
		1f		3f	1/2953
0	1/197	20		40	1/3282
1		21		41	1/3642
2		22		42	1/3985
3		23	1/499	43	1/4364
4		24	1/515	44	1/4749
5		25	1/533	45	1/6056
6		26	1/552	46	1/6823
7		27	1/572	47	1/7621
8		28	1/594	48	1/8538
9		29	1/617	49	1/9585
A		2a	1/643	4a	1/10775
B		2b	1/671	4b	1/12112

C		2c	1/701	4c	1/12303
D		2d	1/735	4d	1/13822
E		2e	1/770	4e	1/15782
F	1/247	2f	1/810	4f	1/17959
10		30	1/854	50	1/20559
11		31	1/904	51	1/23320
12		32	1/959	52	1/26939
13		33	1/1021	53	1/30637
14		34	1/1093	54	1/34722
15		35	1/1175	55	1/40064
16		36	1/1271	56	1/45955
17		37	1/1383	57	1/50403
18		38	1/1518	58	1/55803
19		39	1/1687	59	1/62500
1a		3a	1/1884	5a	1/71022
1b		3b	1/2143	5b	1/78125
1c		3c	1/2311	5c	1/91911
1d		3d	1/2484	>=0x5d	1/97656

5.4. Timing Of communications

The timing of the I2C command varies depending upon the desired shutter speed (integration time).

The integration time will always end at the same point, (approximately 900 uS after the start of the VD pulse and approx 400uS after the end of the VD pulse) and only the starting point will vary.

In order for the new settings to take effect within the current field, the data transmission **must end** within a certain time window. This window extends from 1 ms after the vertical blanking period to the start of the new integration time, as shown in Figure 3.

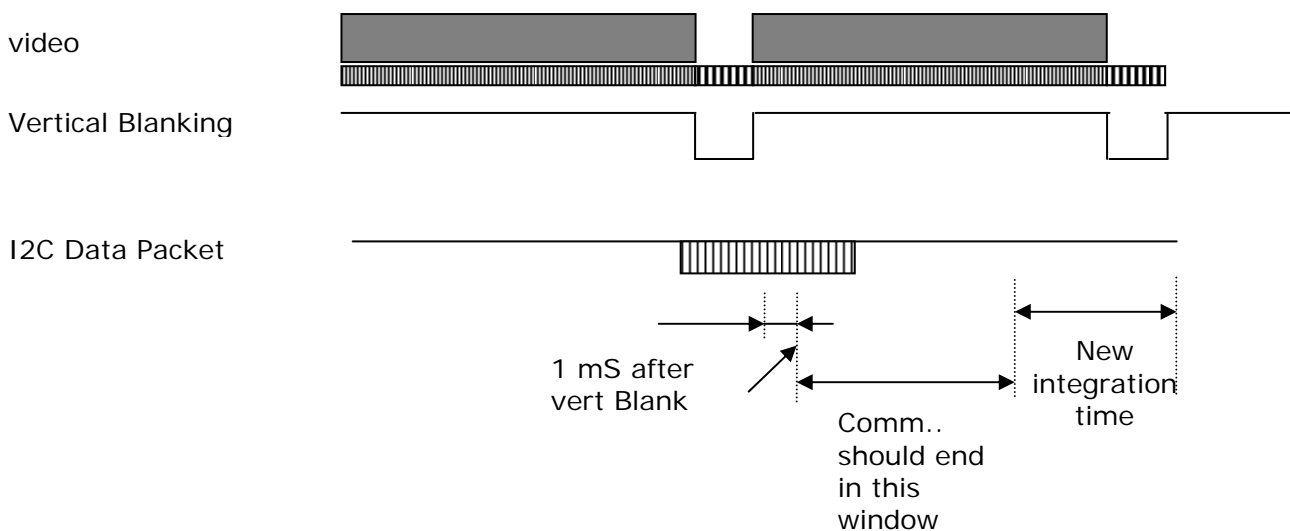


Figure 3. I2C Communications Timing

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It is also essential that the communications do not end within the vertical blanking period or 1 ms thereafter.

In both command modes 1 and 2, if data is not sent within any field, then the shutter speed and gain will remain at the last values sent.

6. Synchronization Modes

7.

The camera has two types of oscillators (depending on the camera model): A crystal for the internal synchronization mode, and an inductor for the external modes.

External synchronization modes:

The module has 4 different synchronization modes to select (depending on the input signals) different lock methods. In Table 4 the 4 different modes can be found. The switching of the mode can be done via I²C software control. For this selection command address 01 must be loaded. Default value is 0x08. This is lock mode 0.

Command register 0x01	Lock Mode
0x08	Default: internal , line-lock, H and V lock
0x01	Asynchronous mode: double pulse
0x02	Asynchronous mode: single pulse
0x04	Field/Frame mode see chapter 4.10
0x00	Hardware control (for more info contact Videology)

Table 4. Synchronization Modes

In the following table, the default synchronization modes can be found:

Locking method	Pin 10 of con. J730	Pin 9 of con J730
Internal lock (X-Tal)	x	x
H & V lock	H-pulse	V- pulse
Line-lock	x	V- pulse

Table 5. Lock Modes by Connection

Polarity of the external signals: active low (negative going).

When no input pulses are applied then the camera is in Internal XTAL mode.

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7.1. Asynchronous Reset

Asynchronous reset means that the external timing has in principal no relation with the timing of the camera and can occur at any moment. At the moment a reset occurs the timing of the camera gets a reset and starts from zero.

At that moment all charge in the photocells of the CCD is dumped. However, the charge in the transport channels remains. This results in the first field generating a non-valid picture. See Figure 4 below:

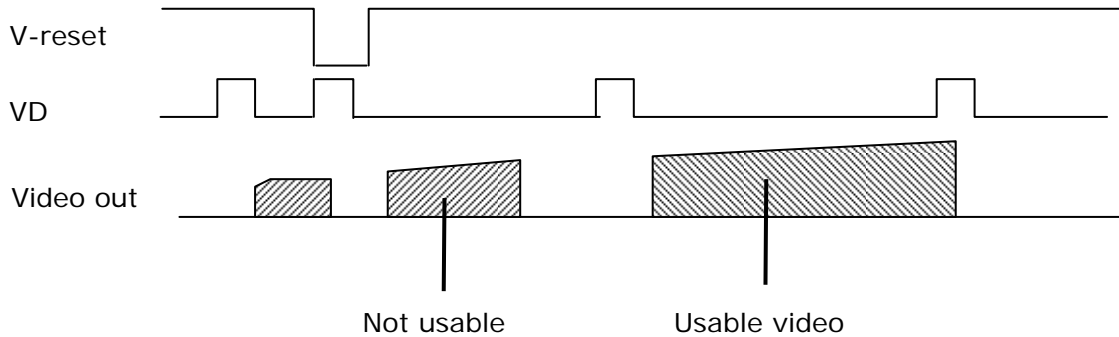


Figure 4. Asynchronous Reset

The above-described system is not a true asynchronous reset. In a true asynchronous reset, you want to be able to use the field directly after the reset pulse and not wait a field.

To avoid this situation the 20/21D389 cameras have an additional logic-timing device on board, which allows the camera to do a true asynchronous reset. The camera has in total 2 different asynchronous lock modes.

The camera has two modes in which the camera generates usable video directly after the reset:

- Single Pulse Reset
- Double Pulse Reset

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7.1.1. Single Pulse Reset Method:

In the single pulse fast reset the integration time is fixed on 1msec. A second pulse on the reset line will have no effect until the previous reset is handled. See Figure 5.

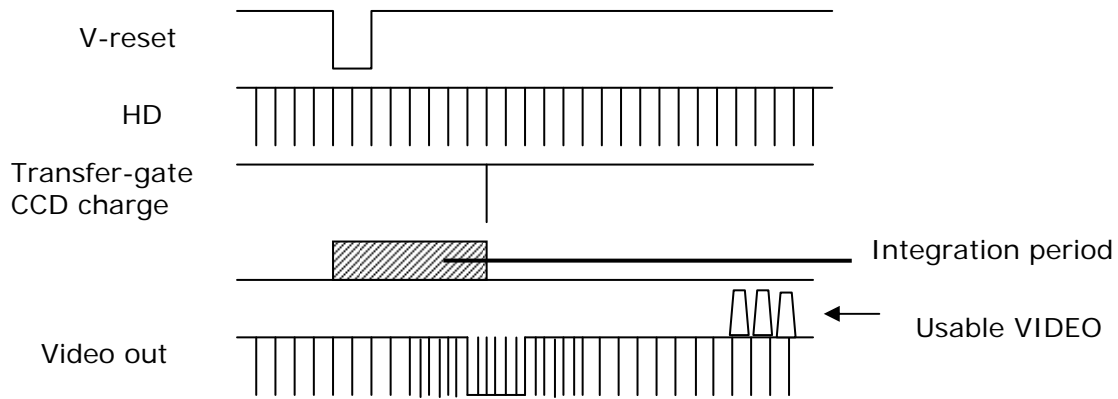


Figure 5. Single Pulse Asynchronous Reset

Integration is started directly after falling edge of the input reset pulse.

Allowing H-lock is important if the camera system always needs to be reset in the same field. By coupling the reset pulse to a H-pulse generator (connecting this also to the camera) the master is in full control when a reset occurs and in which field the reset occurs. Without the H lock this is not possible. Further there is no jitter of 32 microseconds (max).

Note: due to the implementation an extra V-pulse is generated after the reset-pulse. This has no effect on the readout.

7.1.2. Double Pulse Reset Method

With the double pulse reset the user can determine the length of the integration time to a maximum of 1msec. With the first pulse the system is set active and all counters will restart. At the moment the second pulse occurs the CCD starts integrating. See Figure 6:

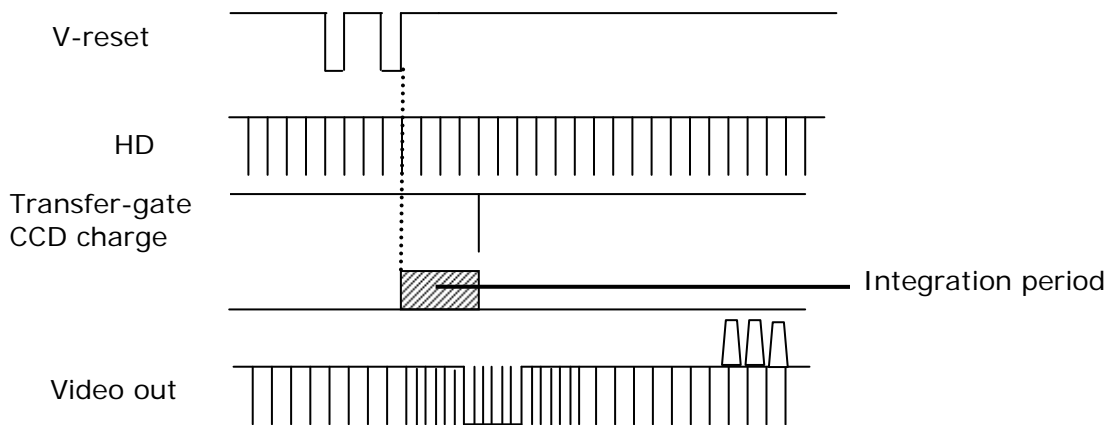


Figure 6. Double Pulse Asynchronous Reset

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7.2. H and V lock

H and V lock means that the camera is synchronized in both the H and V direction. To do this the oscillator is coupled to an external H-pulse and with the V-pulse as with line-lock. The external V-pulse goes to the reset input of the timing chip. This causes a hard reset of the timing chip and the complete camera. When a hard reset occurs, all counters inside the timing generator are restarting again at zero. It is not necessary that the hard reset occur each field or frame. If the camera is already synchronized to the H pulse, this gives a complete timing lock.

The width (active period) of the external V-pulse should be at least 1 line to guarantee that the camera starts in the correct field See Figure 7.

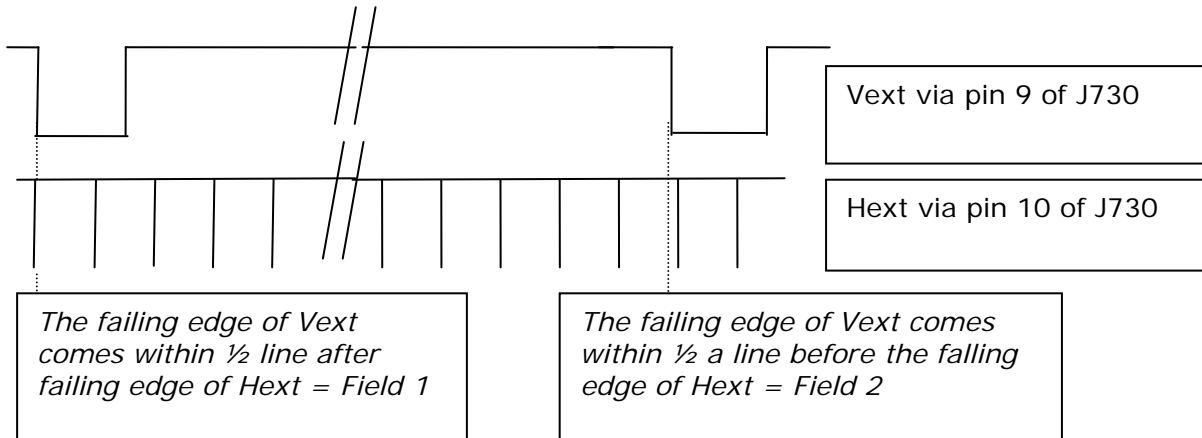


Figure 7. H & V Lock

7.2.1. Line lock

Line-lock means that a 50 or 60 Hz (CCIR or EIA) pulse is supplied to the camera. The external V-pulse and the internal V-Pulse are compared with each other. The frequency (or phase) of the camera oscillator is adjusted until the two V-pulses are locked. By feeding the external V-pulse (via pin 9 of connector J730) to the camera the camera is running in the line lock mode.

Allowing H-lock is important if the camera system always needs to be reset in the same field. By coupling the reset pulse to a H-pulse generator (connecting this also to the camera) the master is in full control when a reset occurs and in which field the reset occurs. Without the H lock this is not possible. Further there is no jitter of 32 microseconds (max).

7.2.2. Sync-lock

In fact this lock is comparable with H&V-lock. The camera is synchronized in both the H and V- direction. To do this now the Composite Sync. Pulse is connected to pin 10 of connector J730 (in stead of H-pulse). Also figure 6 applies to this situation.

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8. Gain control

8.1. AGC

The camera has an automatic gain control in the default mode. This function is responsible for the output signal remaining constant at a certain level. If the camera is pointed to a gamma reflection chart 0.45 the output should be 1Vp-p. This control circuit works with an integrator. This integrator generates from the video signal a signal that corresponds with the average value of the signal. This average is compared with an internal reference and depending on the outcome of the gain will increase or decrease.

8.2. Manual Gain Control

If the automatic gain control should be switched off, send via the I²C interface to command register 0x07 a value of 0x80 for fixed gain is 0dB. By sending 0xFF the gain goes to its maximum level. All values above 0x80 are fixed values. Below the gain control is automatic.

8.3. Gamma

A camera has a gamma function to correct the non-linear behavior of the monitor CRT. The gamma curve of the camera is 0.45. With this gamma setting the monitor is able to display the scene as we see it with our eyes.

However if the camera video signal is processed for pattern recognition this gamma function is often not wanted. To make this possible the 20/21D389 has a gamma option, this can be selected also via the I²C serial interface. In case of sending 0xFF to command register 0x02 the gamma factor is 1. By putting in 0x00 (default) gamma is 0.45.

8.4. Back Light Compensation

The camera has a default setting of standard back light compensation (BLC) on. This means that for the electronic iris circuit only the main part of the scene is taken into account to determine the level of the CCD output (see Figure 8) When fixed shutter speeds are used this function has no effect

Sometimes it can be required that the complete image should be used to determine the CCD output level. This function can be addressed via command register 0x03.

The Back Light Compensation is fully programmable:

Size of the window and position of the window can be programmed. Also weighting factors (relation between the BLC window and rest of the image) can be programmed.

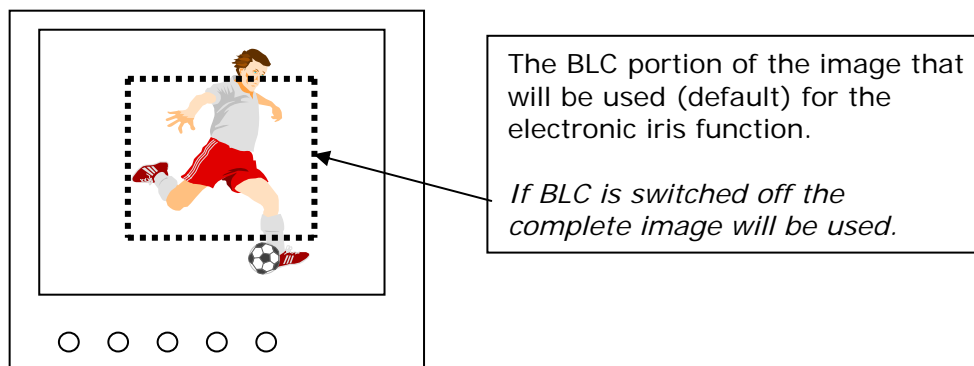


Figure 8. BLC

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9. Spectral Response

The CCD is the eye of the camera. It converts light into an electrical signal that will be turned into a video signal by the processing of the camera. However the camera is not sensitive for all types of light and has a sensitivity peak at 550 nm.

The spectral curve of the 20/21D389 ranges from the visual part of light to the near infrared area (1100 nm). Due to the use of Sony Exview CCD[®] the IR sensitivity is improved drastically. Only filters may change the response. The complete curve is shown in Figure 9:

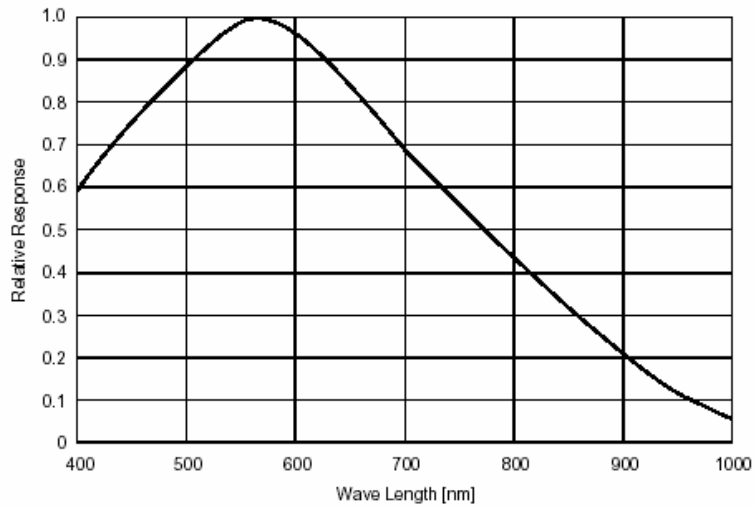


Figure 9. Spectral Response

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10. Scan Mode

The camera runs normally in the interlaced mode according to the CCIR or EIA standard. This means that a full picture (frame) is built up out of two half pictures (fields) who are shifted half a line compared to each other. For a graphical view see 10.

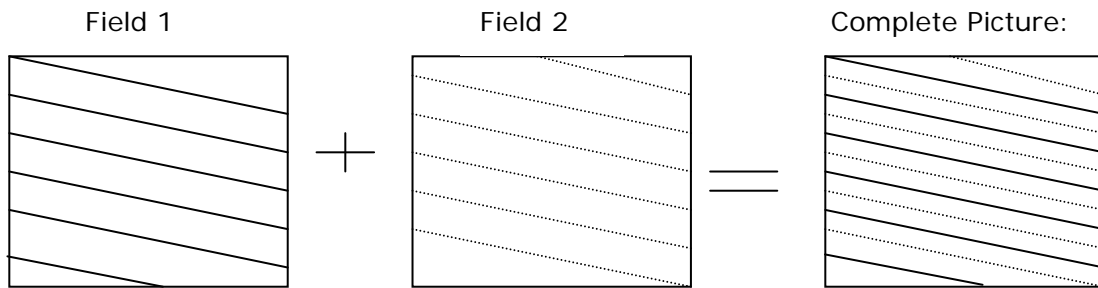


Figure 10. Interlaced Picture

This means that every 40ms (for CCIR) or 33.3ms (for EIA) the camera has generated a complete picture.

However sometimes the application does not require the high vertical resolution, but desires to have the same information in each field (without the half line shift between the fields). In that case the two fields are identical to each other. See Figure 11.

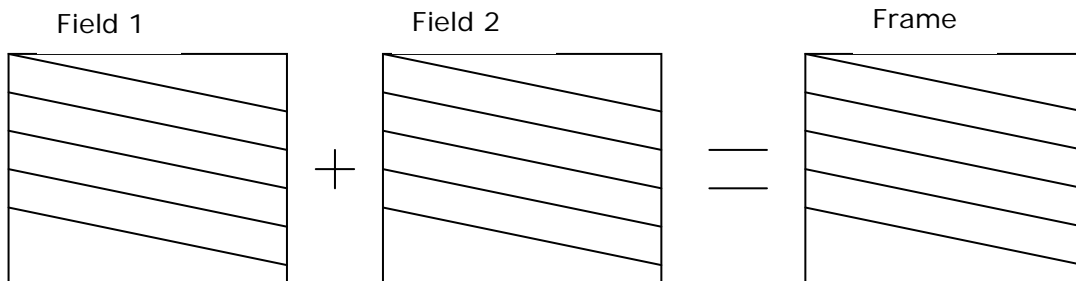


Figure 11. Non-Interlaced Picture

In figure 10 it can be seen that the vertical resolution is less compared with the interlaced mode (see figure 9), but that the fields are identical with each other and therefore the frame rate is increased (doubled).

To put the camera in the non-interlaced mode send 0x0F to Command register 0x0A.

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11.Field/Frame Integration

Most cameras work in a **field integration** mode. This means that the complete CCD is read out after every 16.6 msec. (EIA) or 20 msec. (CCIR). However, the first field that is read out of the CCD is different from the second field. This produces interlaced video. To generate the two fields the vertical lines in the CCD are combined as follows:

Field 1; lines 1 and 2, lines 3 and 4, lines 5 and 6, etc.

Field 2; lines 2 and 3, lines 4 and 5, lines 6 and 7, etc.

As you can see each line is used twice, once in each field. Due to this the CCD has reduced resolution and only has vertical resolution of 415 TV lines.

The 2/21D389 can be put into a **frame integration** mode, which will increase the vertical resolution of the CCD. With this mode every line is exposed for twice the field integration period (full frame) with odd and even lines read out separately at the field rates. The video output is still interlaced and may be displayed on a standard CCTV monitor, however the vertical resolution is increased to 485 TV lines.

A disadvantage to this method of integration is that due to the longer exposure time fast moving objects within the scene may be blurred. Limiting the integration periods by using fixed shutter speeds may help reduce this blurring, however sensitivity will be reduced.

The standard mode of the 20/21D389 is the **field integration** mode. To put the camera into the **frame integration** mode:

Make bit 2 of command register 0x01 → 1 (0x40, 0x01 data: 0x04). The 2 Lsbits are for the lock mode.

Or put in command register 0x01 → 0x00. Make pin 4 of the digital connector low.

11.1. Frame Rate

The camera is normally working according to the EIA or CCIR standard. However the components are selected in such a way that by increasing the main clock frequency also the vertical frequency can be increased up to 75 Hz. To achieve this the new frequency of the crystal should become:

camera	Vertical frequency: 75 Hz
20D389 (EIA)	35.79545 MHz
21D389 (CCIR)	42.5625 MHz

Table 6. Crystal Frequency

The crystal should be a standard type (fundamental).

12.CPLD Flexibility

The CPLD can be programmed to perform extra functionality on request.

For sufficient volume applications, the camera can be customized. Please contact Videology U.S.A. or Europe to discuss qualification.

One example of this capability is the extended integration feature described in section 4.13.

13.Extended Integration

The camera has the capability of an extended, externally controlled integration time. Depending on the cooling precautions taken, the integration time can be extended to ten seconds or more. The resulting image should then be stored in frame memory for display or processing.

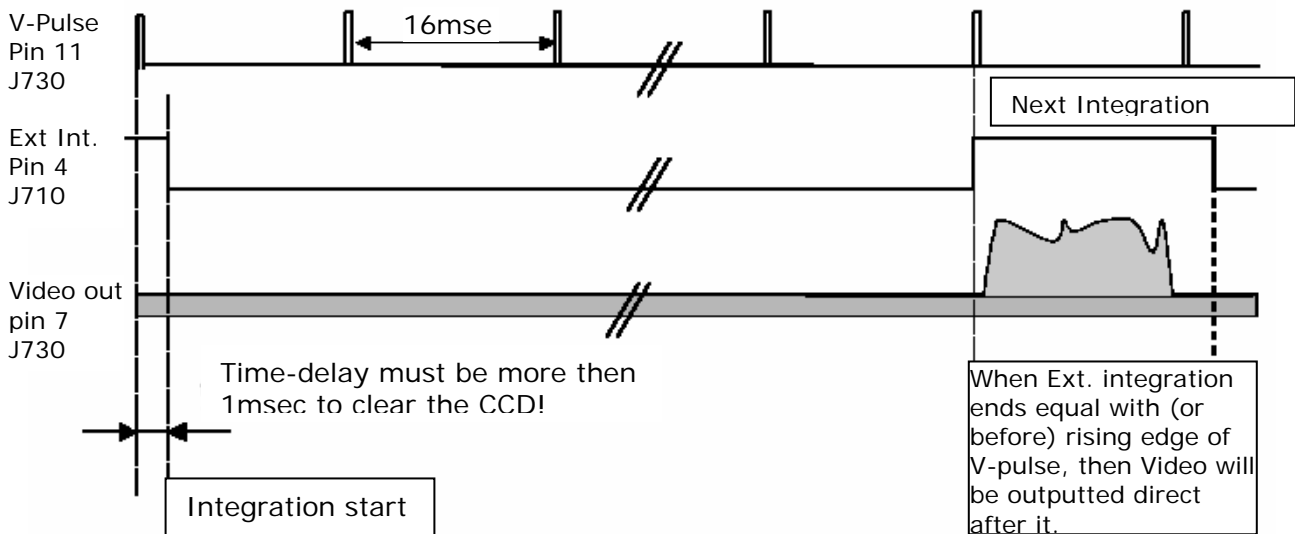
Camera settings:

Gain should be fixed [command 0x40- address 0x07 data 0x80 (for minimum)]

Shutter to be set to 1/50, in this case the CCD will be cleared (command 0x40- address 0x06 data 0x01).

Pin 4 of J710 must be pulled down to start integration.

Figure 12. Extended Integration



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14. Software Control

14.1. Camera Software Protocol

The camera has a serial control interface via three wires:

- Data wire
- Clock wire
- Ground wire

This interface operates similar to the I²C-protocol.

Data, address and registers are all 8-bit words. The data and clock signals are shown in Figure 13.

The maximum speed limitation is 10kHz. The minimum speed should be higher than 100Hz. There should be a waiting time of at least 10m sec, between the write actions to the EEPROM.

Further a wait time is required between the commands, so that the internal communication camera has the time to do the required internal communication. The delay time between the commands should be at least 2msec.

When sending a read command, the last acknowledge of the command block from the camera has a delay of maximum 2msec. During this delay the camera gets the required data from the EEPROM. The sender has to wait until this acknowledge is received, otherwise communication will fail.

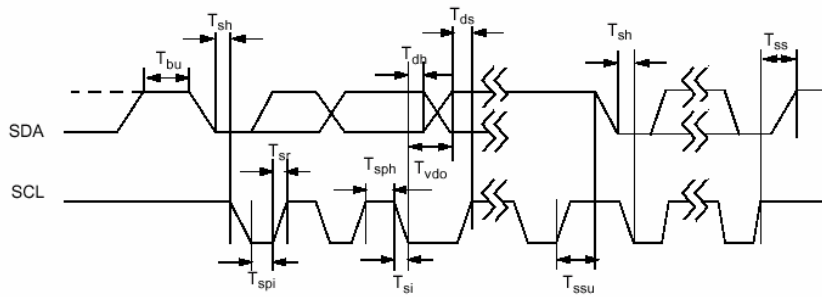


Figure 13. Communication Protocol

Standard I²C address camera: 0x70

The communication-structure contains a Command block and a Data block.

Command block:

<START> <cam_address>ackn<acces_mode>ackn<device>ackn <register>ackn<STOP>

Cam_address	Acces_mode	device
Standard=0x70*	00=write to camera 01=read to camera 09=dump (write) EEPROM**	00=encoder 30=DSP 40=commands a0,a2,a4,a6= EEPROM

Data block(if acces_mode !=09, accesmode is not configured as dump-mode) :

<START><cam_addressR/W>ack<data>ackn/Nackn***<STOP>

Cam_address	Data:
Access mode=00: 0x70	Write data to camera with ackn

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Access mode=01: 0x71	Read data from camera with NOT ackn.
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*The address can be changed. In address 0xa0 of the EEPROM: 0xa2 is the address of camera stored. Camera can get new address if customer wants/needs!

**Special mode to access EEPROM faster for production. Block writing is possible so that the camera address is not required each time. First both passwords have to be given before access is allowed!

***NOT acknowledge means: master send a clock low→high→low as with a normal acknowledge, but camera may not respond by pulling data line low. This must be checked otherwise the number of bits are not correct!

Example 1 Write Action:

Set white balance mode to Push to White, this means:

Command 40; register 00 and data 03:

Write action:

Command-block:

<start> 70 ackn 00 ackn 40 ackn 00 ackn <stop>

datablock:

<start> 70 ackn 03 ackn

description: camera-address 70, access mode write, device 40 (command), register 00,

datablock: write address 70 , data 03.

Example 2 Read Action:

Command 40; register 00 and read data :

Read action:

Command-block:

<start> 70 ackn 01 ackn 40 ackn 00 ackn <stop>

data block:

<start> 71 ackn Nackn

description: camera-address 70, access mode read, device 40 (command), register 00,

data block: read address 71 , camera will sent data.

14.2. Camera Configuration:

The device addresses have two values, one for read the other one for write. The difference is that the last bit (LSB) is set to one. For the communication the next device addresses are available:

Device	Device writeaddress
DSP	0x30
Commands	0x40
EEPROM page 1	0xa0
EEPROM page 2	0xa2
EEPROM page 3	0xa4
EEPROM page 4	0xa6

Table 7. Device addresses

It is not possible to read from the DSP. The DSP is a write only device.

Don't write to the DSP because it can make the camera non-functional.

EEPROM pages 3 and 4 are protected by a password! The normal user may not have access to these two pages since the back up settings and production date is saved in here.

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The DSP settings are directly mapped on EEPROM page 1.
The camera will recognize several commands. Often these will be a combination of several internal commands to fulfill a certain task. To send commands to the camera:

First - the device number 0x40 has to be send.
Second - the command self (at the place normal the address will be found) must be send.
Third - the data.

14.3. I²C Address

The camera has an I²C address so that more than one camera can be connected to I²C bus.

The camera default has address 0x70.

In case the user may have forgotten the new address he/she can reset it back to the factory default by connecting pin 16 of the micro processor (port 0.5, test-point available on board) to ground:

Connect to ground for at least 4 seconds.
The I²C address is stored in the EEPROM page 2 address 0x90 (hex).
To change this address one should write: device 0xa2; address 0x90; value 0xXX.
XX is free to choose. With this method you can have 256 different I²C addresses for the camera.

With device 0xa3 one can read the value.

14.4. Communication Reset

If the communication is interrupted, the microprocessor will automatically reset the communication lines.

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14.5. Command Registers

To address the command 40h has to be send. Direct after that the command register and value. The following commands can be executed.

For more detail please see the readme.doc which is with the SW-package.

Command	Command number	Data range
reserved	0x00	Not used
Lock modes	0x01	0x08: Default mode: Internal (no input on HEXT & VEXT) Line lock (only vertical pulse on VEXT) H&V lock (H&V pulse on VEXT & HEXT) 0x00: Hardware mode (lock control via pins Mode1-LV and Mode 2-LV) 0x01: A-synchronous Reset with double pulse 0x02: A-synchronous Reset with single pulse 0x03: Composite Sync-lock (Composite Sync signal connected to HEXT) 0x04: Frame mode
Gamma	0x02	0x00: gamma is 0.45 (default) 0xff: gamma is 1
Back light comp.	0x03	0x00: BLC on 0xff: BLC off
RESET: load defaults	0x04	0xac: reset load default values
Mirror mode	0x05	0x00=normal, 0xff=mirror
Shutter mode	0x06	0x00: electronic iris 0x01: 1/50 or 1/60 sec 0x02: flickerless 0x03: 1/250 0x04: 1/500 0x05: 1/1000 0x06: 1/2000 0x07: 1/10000 0x08: 1/20000 0x09: 1/50000 0x0a: 1/100000 0x0b: 1/25 or 1/30 sec (intermittent frame readout) 0x0c: 1/12.5 or 1/15 sec (intermittent frame readout) 0x0d: 1/6.5 or 1/7.5 sec (intermittent frame readout) 0xff: hardware control 8 values, via PROG-MODE pins connector J710.
Gain control	0x07	0x00= auto mode 0x80= fixed gain minimal 7 LSB's are fixed gain: The MSB indicates fixed gain 0xff= fixed gain maximal gain
Non-interlaced	0x0a	0x00: interlaced 0x0f: non-interlaced 0xff=hardware control via PROG-MODE 4
Edge enhancement	0x0b	0xc0 edge enhancement off gain range 0x00 up to 0x1F

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Standby	0x0c	0x00= DSP active, 0xff DSP standby after a power down and up the camera will start , does not stay in standby.
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BLC window can be programmed for special light situations:

Size BLC window	0x08	64 windows can be defined over the whole active pixels. This means that for PAL: H = 94 pixels and V = 72 pixels ; For NTSC: H= 96 pixels and V = 62 pixels. Size H x V 0x00 1H x 1V 0x01 1H x 2V 0x02 1H x 4V 0x03 1H x 8V 0x04 2H x 1V 0x05 2H x 2V 0x06 2H x 4V 0x07 2H x 8V 0x08 4H x 1V 0x09 4H x 2V 0x0A 4H x 4V 0x0B 4H x 8V 0x0C 8H x 1V 0x0D 8H x 2V 0x0E 8H x 4V
Position BLC window (9 window positions possible)	0x09 (See also figure below)	0x00 center 0x01 Top left 0x02 Top center 0x03 Top right 0x04 Center left 0x05 Center right 0x06 Bottom left 0x07 Bottom center 0x08 Bottom right

Table 8. Command Registers

1	2	3
4	0	5
6	7	8

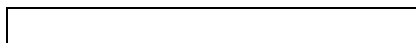


Figure 14. BLC position

The BLC weighting factor can also be programmed. The value of this factor (which in fact is a number which determines how the ratio between window and the rest of the image is calculated) is stored in EEPROM.

The EEPROM address is 0x98 on page A2/A3.

The command settings are stored in side the memory of the camera. After a power down the camera will come up with the last used settings again (except standby).

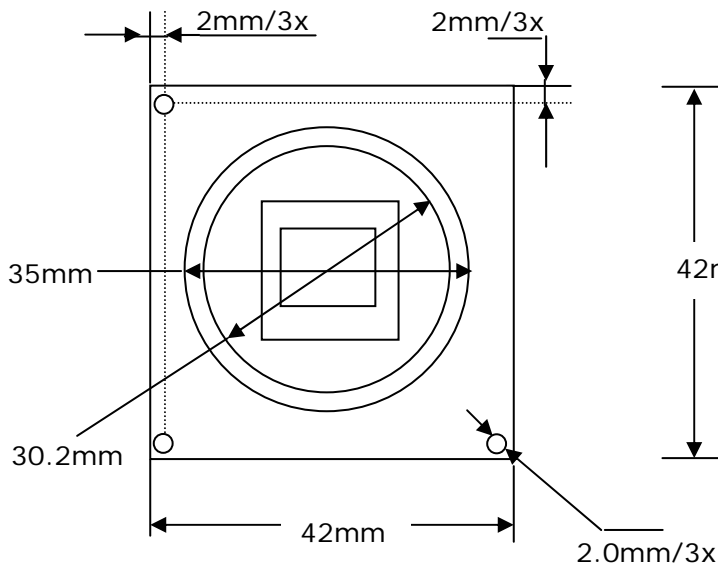
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15.Mechanicals/Connectors

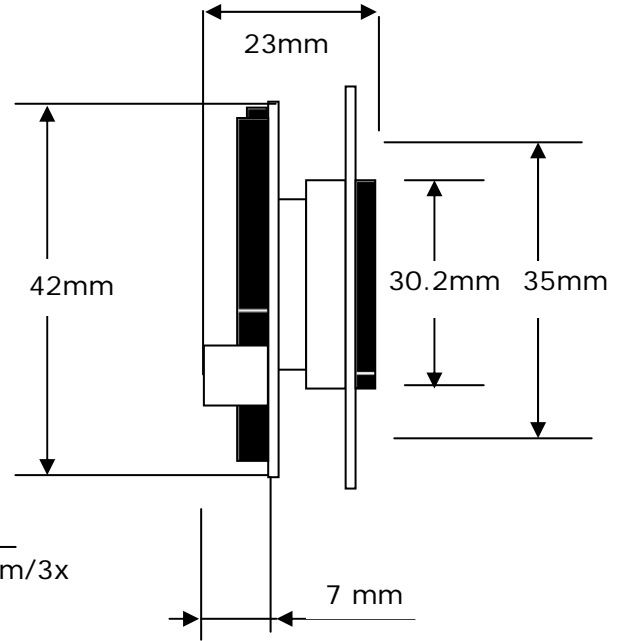
This chapter gives the mechanical information about the 20/21D389. This mechanical information also includes connector information.

15.1. Board Outline

Front View - CS Mount

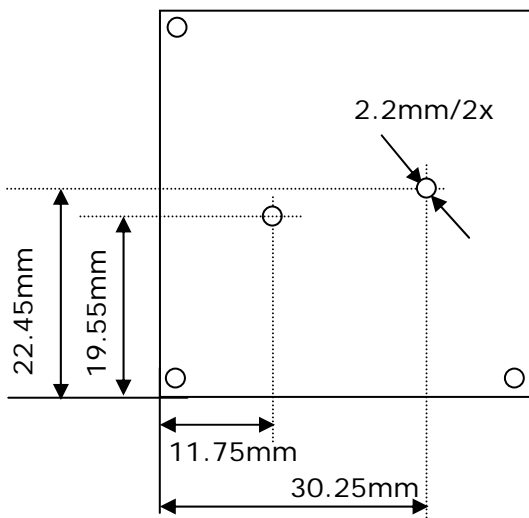


Side View – CS mount

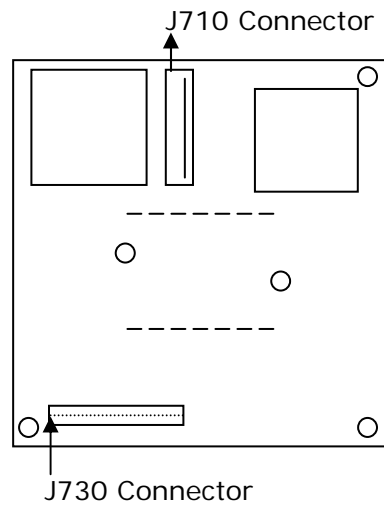


Board lens optional available

Front View – Board Mount



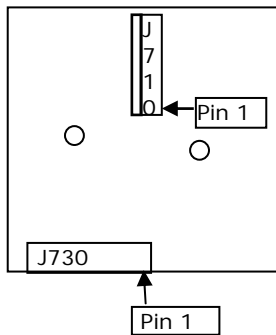
Back View – No Mount



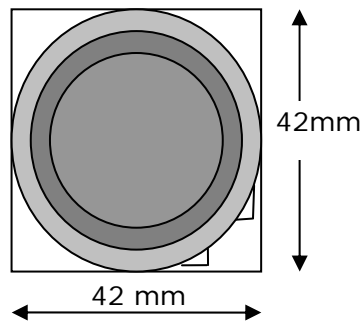
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15.2. Connectors

The camera has one connector that can be used as interfaces for the user of the camera. Both are located at the backside of the camera (see figure below).



Backside of camera



Front side of camera

J730 is a 13-pole JST connector, type BM13B. J710 is a 24 pole JST flat foil connector, type 24FLT-SM1-TB. Pin connection:

Pin no.	Pin function J730	Pin no.	Pin function J710 flat foil connector
1	Horizontal Sync out	1	Ground
2	GND	2	SCLOCK I2C
3	+12V IN	3	SDATA I2C
4	Not used.	4	MODE3-LV (reserved for Extended Integration see chapter 4.1213)
5	GND	5	MODE2-LV LM1 hardware control lockmodes
6	NOT CONNECTED	6	MODE1-LV LM0 hardware control lockmodes
7	CVBS (Luminance out)	7	MODE0-LV (reserved for Frame mode)
8	NOT CONNECTED	8	Pixel Clock
9	VEXT (vertical sync in)	9	Ground
10	HEXT (horizontal sync in)	10	PROG-MODE4
11	Vertical Sync out	11	Y7 msb-bit luminance digital out
12	SDATA I2C	12	Y6
13	SCLOCK I2C (black wire)	13	Y5
		14	Y4
		15	Y3
		16	Y2
		17	Y1
		18	Y0 lsb-bit luminance digital out
		19	Ground
		20	Vertical-SYNC out
		21	PROG-MODE2
		22	PROG-MODE3
		23	Horizontal-SYNC out
		24	PROG-MODE1

Please note: connector J710 has been changed with respect to previous models!

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16. Specification

Electrical		
Image device		1/3" Inter Line Exview CCD
Number of active picture elements		PAL: 752 (H) x 582(V) NTSC: 768(H) x 492(V)
Horizontal resolution		>560 TVL
Sensitivity		< 0.001 Lux (30 IRE) F1.2 3200K, lens transmission 80%, scene reflection 75%
Signal to noise ratio		>48 54 dB (AGC off)
Gain control		Automatic 36 dB (default) Manual via software
AGC detection mode		Average (default)
Scan mode		Interlaced (default), Non-interlaced selectable via software
Gamma		0.45 (default) selectable via software
Back light comp.		Default off, selectable via software
Contour enhance		Default on
Iris control		Electronic (default) Fixed Shutter speeds (selectable) 8 values (table 2)
Synchronization		Internal (X-tal), H&V lock, line lock. Asynchronous reset, sync lock
Outputs:	Video	1 Vp-p CVBS 75 Ohm
	Digital	8-bit digital luminance output signal plus pixelclock (cmos output, 3V3 pulse)
	Synchronization	H and V output; (cmos output, 3V3 pulse)
	Iris	1 Up-p (for auto iris lens)
Inputs:	power	+12V tolerance +3V /- 4V
	Vext	Connection for V-pulse for Line-lock or H&V-lock (cmos input, 3V3 pulse)
	Hext	Connection for H-pulse for H&V-lock or comp. sync for sync-lock. (cmos input, 3V3 pulse)
Supply Voltage		12V DC + 3V/- 4V
Power consumption		< 1.5 Watt

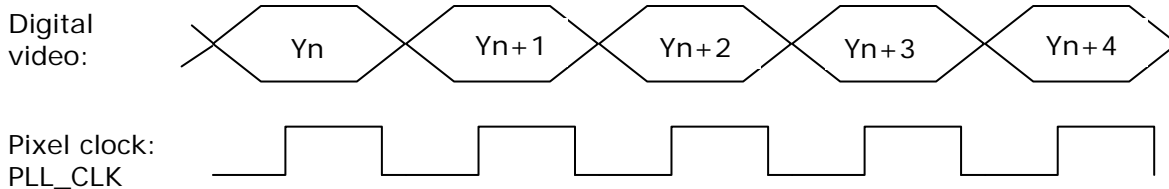
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Mechanical		
Lens mount		CS-mount, optional C-mount with interface ring. Optional without lens mount Optional with Board lens mount (M12)
Image format		1/3"
Dimensions		42mm x 42mm x 13.4mm (LxWxD) without lens
Interface		Board connectors
Interface cables		13, 10cm length unterminated wires
Environmental		
Ambient temperature	Operational	-15 ⁰ to +55 ⁰ Celsius
	Storage	-25 ⁰ to +70 ⁰ Celsius
Ambient Humidity	operational	20 to 93%RH
	storage	Up to 98% RH
Lifetime		MTBF >150000
Approbation		TBD
Packaging		Modules will be packed in ESD safe foil, together with user manual in carton box.

17. Digital Output

Format for the 20/21D389 monochrome module:

The output bus is 8 bits wide.



The PLL_CLK clock rate is:

CCIR : 14.1875Mhz (Field rate 50Hz)
EIA: 14.318 Mhz (Field rate 60Hz)

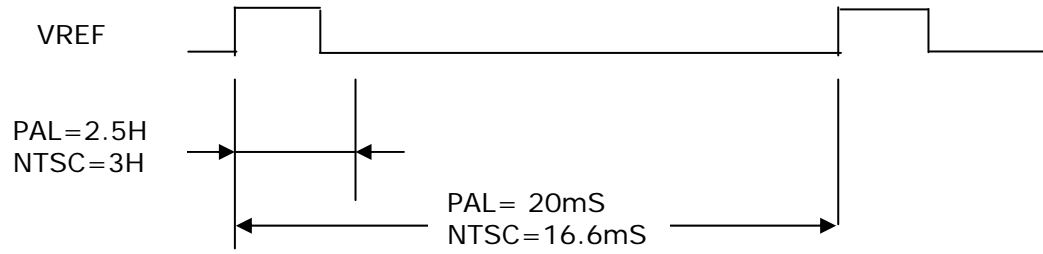
Beside these pixel related signals on the output connector there is also an H sync out signal available as sign of the Horizontal active video period. The polarity of this signal is programmable.



Above is the Horizontal pulse (equal to active pixel data) one must set register 0x03 of DSP to value 0x58 to obtain this (active low) pulse. In normal mode (H = active high) it is programmed to 0x38 (this is mostly used for H-and V-lock).

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In vertical direction a V sync out signal is available. This signal has a positive polarity. The signal is present during the vertical serration pulses.



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18.Contact Information

For technical assistance with this product, please contact the supplier from whom the product was purchased.

For OEM inquiries, contact Videology Imaging Solutions:

North / South America:	Europe:
Videology Imaging Solutions Inc. 37M Lark Industrial Parkway Greenville, RI 02828 USA Tel: (401) 949-5332 Fax: (401) 949-5276	Videology Imaging Solutions Europe Neutronenlaan 4 NL-5405 NH Uden, Netherlands Tel: +31 (0) 413 256 261 Fax: +31 (0) 413 251 712

Please visit our website at: <http://www.videologyinc.com>

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