VIDEOLOGY®

IMAGING SOLUTIONS INC.

Application Note

20D476/21D476 (M-12 Mount)
20D479/21D479 (CS Mount)
High Resolution Color Board Camera

Information may change without notice.

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Videology Imaging Solutions, Inc. USA
37M Lark Industrial Parkway
Greenville, RI 02828
Tel: 401-949-5332
Fax: 401-949-5276

Videology Imaging Solutions, B.V. Europe
Neutronenlaan 4
NL-5405 NH Uden, Netherlands
Tel: +31 (0) 413-256261
Fax: +31 (0) 413-251712

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1. Introduction

The 20/21D47X is a high-resolution color camera module with a CS-mount lens interface. The basic module is a single board camera with a high resolution CCD and several extra features. The state of the art components in the 20/21D47X provide superb image quality. Multiple features and small size of 42 x 42 mm allow for usage in almost every application.

This document is written to give technical background on specific features of this camera.

2. History

Revision	Issue Date	Reason	CN#
Rev A	20-11-2002	Initial	N/A
Rev B	01-04-2003	New protocol	N/A
Rev C	04-09-2003	Hardware camera change	04-0126
	09-24-2003	Embedded software change	
	01-28-2004	Add digital output format	
Rev D	06-13-2004	Shutter speeds changed	04-0162
Rev E	07-05-2007	Section 4.2 Shutter speeds edited	07-0145
Rev F	12-05-2008	Photograph and dimensional drawings changed	08-0189

3. Features

Utilized on all 20/21D47X main single camera boards.

Standard basic features include:

- CCD horizontal 768/752 pixels, (horizontal) resolution 490 TVL
- Integrated Auto Exposure Control (Iris/AGC)
- Edge enhancement
- Fixed gamma (0.45)
- Sensitivity 50 IRE lens F1.2: <0.5 Lux

Additional features of the 20/21D47X main board are:

- Possible outputs include:
- CVBS
- Y/C (S-VHS) / YUV
- RGB output (video-based)
- Synchronization modes:
- Internal X-tal locked
- External line lock
- Fixed shutter speeds (8 values including flicker-less)
- Manual gain control (via I^2C control software)
- Back light compensation on/off (default on)
- Supply voltage +12V DC (+ 3V / - 4V)
- Push Lock White Balance
- Mirror mode
- Computer controllable

Camera-modules are also available in housing.
The model numbers are: 20D779 (NTSC), 21D779 (PAL)

Software to control the camera is available on request.

3.1. Options Available On Request:

- High contrast mode
- Multiple false color modes

4. Camera Module Functionality

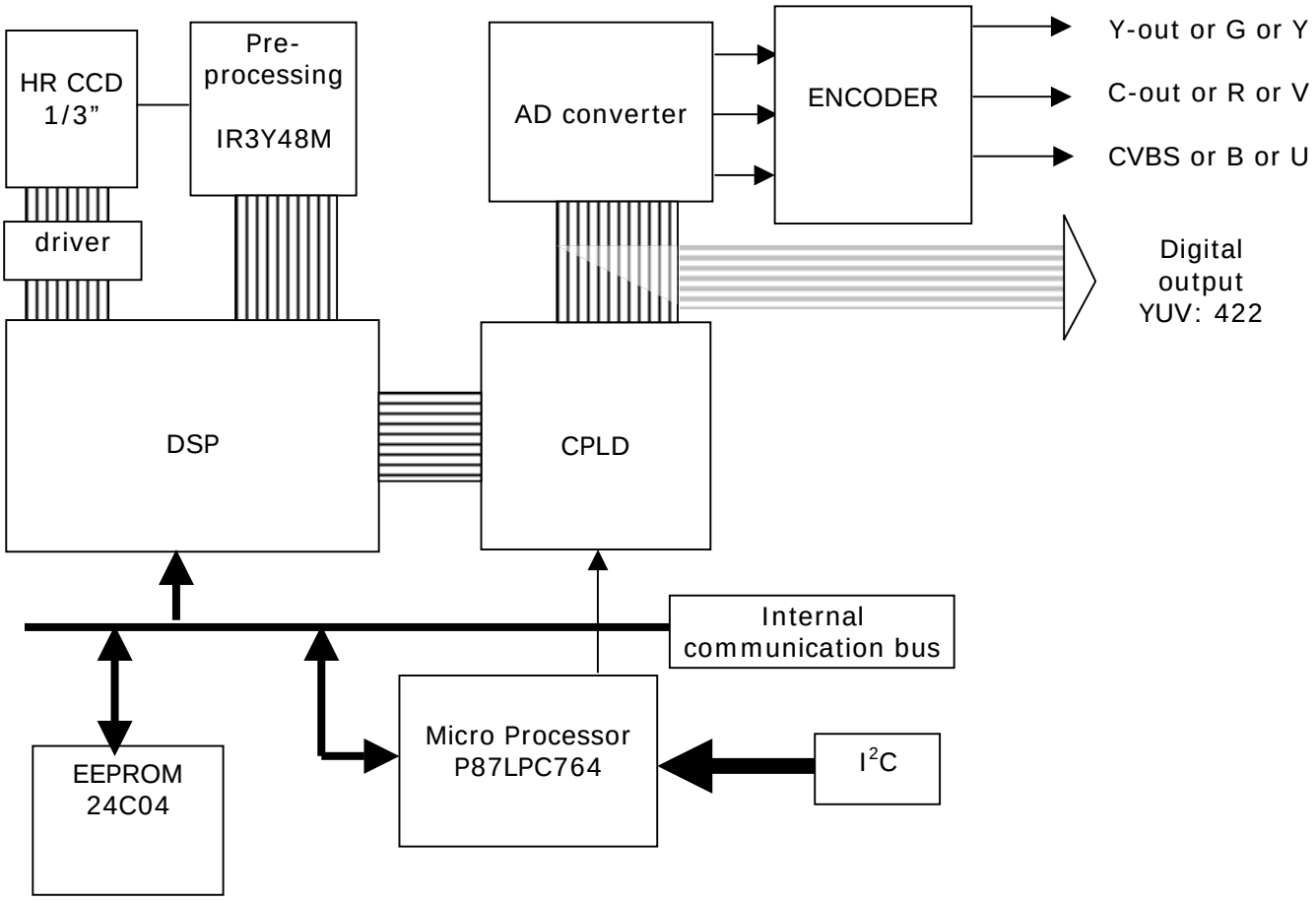


Figure 1. Block diagram

A main advantage of this camera is the manner in which the digital output is programmed. The digital output of the DSP is be manipulated by the CPLD which is a programmable device and not subject to the limitations of hardware. Extra functionality can be programmed on request. This makes the 20/21D47X a “smart camera”.

The following basic functions are possible with the 20/21D47X camera-module:

4.1. White Balance Mode:

Via software you can select 2 fixed modes or the Auto White balance mode.

Also you can select via software the “Push to Set” WB mode (which is in fact also a fixed mode). The white balance then is set via pressing (or via software) the button on the back and pointing the camera to a white scene.

4.2. Fixed Shutter Speeds

In default mode, the camera operates in the electronic iris mode. This means the output of the CCD, which is dependent on the light intensity, is controlled by the electronics of the camera and not the mechanics of the lens.

To do this, the camera has an OFD pulse. When this OFD pulse is active (Low), (see Figure 2) the charge that is built up in the photo diodes is dumped into the substrate of the CCD.

So after each OFD pulse the accumulation of the charge in the photocells of the CCD start from zero. The amount of signal out of the CCD is dependent on the light intensity and the time that the charge can build up (the period during which no OFD pulse is present).

Therefore, by measuring the output of the CCD and comparing it with an internal reference it is possible to control the level of the signal out of the CCD (within a certain tolerance).

However, sometimes it is preferred that the shutter is fixed and not automatic. An example where using a fixed shutter is beneficial is if there is a very fast moving object in the scene.

The longer the integration time (the period that no OFD pulse occurs, max 1/50 sec for PAL and max 1/60 sec for NTSC) the more blurred the image will appear due to the movement of the object during the integration period.

To prevent this the camera has 8 fixed shutter speeds (see Table 1). To switch the electronic iris off there are two options: either via I^2C software control or via hardware control. In the last mode it is required that the module gets a special software setting (command setting 06h should be loaded with FFh to force the camera in hardware control).

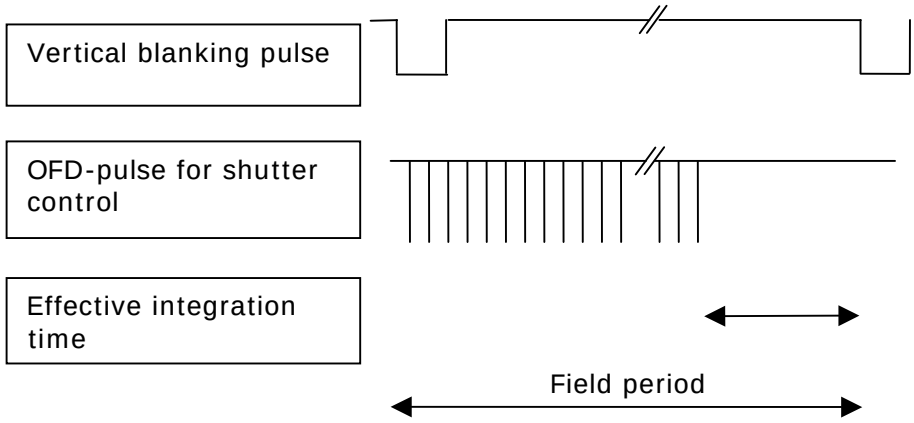


Figure 2. OFD Shutter Control

Table 1. Fixed Shutter Speed

Shutter speed		Command address 06h	PM1	PM2	PM3	PM4
20D47X (NTSC)	21D47X (PAL)					
1/60 sec (max)	1/50 (max)	0xff	high	low	low	low
1/100 sec (flickerless)*	1/120 sec (flickerless)*	0xff	high	low	low	high
1/250 second		0xff	high	low	high	low
1/500 second		0xff	high	low	high	high
1/1000 second		0xff	high	high	low	low
1/2000 second		0xff	high	high	low	high
1/10000 second		0xff	high	high	high	low
1/20000 second		0xff	high	high	high	high
Auto mode		0x00	x	x	x	x
1/60 sec (max)	1/50 (max)	0x01	x	x	x	x
1/100 sec (flickerless)*	1/120 sec (flickerless)*	0x02	x	x	x	x
1/250 second		0x03	x	x	x	x
1/500 second		0x04	x	x	x	x
1/1000 second		0x05	x	x	x	x
1/2000 second		0x06	x	x	x	x
1/10000 second		0x07	x	x	x	x
1/20000 second		0x08	x	x	x	x
1/50000 second		0x09	x	x	x	x
1/100000 second		0x0a	x	x	x	x
1/30 second	1/25 second	0x0b	x	x	x	x
1/15 second	1/12.5 second	0x0c	x	x	x	x
1/7.5 second	1/6.25 second	0x0d	x	x	x	x

Flickerless means that a PAL camera can be used in a 60 Hz (or a NTSC camera in a 50 Hz) light environment without flickering.

In table 1 “low” stands for connect connector pin to ground and “high” for connector pin **open** or connected to +3.3V.

PM1, PM2, PM3 and PM4 (PROG-MODES) are available on connector J710 but can also be fixed too low level (default high level) on camera board by populating resistor (shape 0402) R621 for PM1, resistor R625 for PM2, resistor R627 for PM3 and resistor R632 for PM4. Resistor mounted is equal to “low”. Resistor not mounted is equal for “high”.

The default factory setting is that command register is loaded with 0x00 and all connector pins are High (open).

The lower three lines in the table are special modes. When using the extended integration times (1/30, 1/15 or 1/7.5 second) you will have to consider that these integration times will exceed normal video timing. This means that this will result in blinking video due to the missing fields. This mode is used to increase sensitivity of the camera even more. To get full advantage of these modes you need to use video-memory (to get continuous video) or use a capture board.

4.3. Synchronization Modes

The camera has two types of oscillators (depending on the camera type): A crystal for the internal synchronization mode, and an inductor for the external modes.

4.3.1. External Synchronization Modes:

The module has 3 different synchronization modes to select from. These are internal synchronization and external synchronization. In table 2 the 2 different external lock modes can be found.

In the following table (Table 2), the default synchronization modes can be found:

Table 2. lock modes

Locking method	Pin 10 of conn. J730	Pin 9 of conn J730
Internal lock: X-TAL	x	x
H & V lock	H-pulse	V-reset pulse
Line-lock	x	V- pulse

Polarity of the external signals: active low (negative going).
When no input pulses are applied then the camera is in Internal Lock mode (X-TAL).

4.3.2. H and V Lock

H and V lock means that the camera is synchronized in both the H and V directions. To do this the oscillator is coupled to an external H-pulse and with the V-pulse as with line-lock. The external V-pulse goes to the reset input of the timing chip. This causes a hard reset of the timing chip and the complete camera. When a hard reset occurs, all counters inside the timing generator are restarted again at zero. It is not necessary that the hard reset occurs on each field or frame. If the camera is already synchronized to the H pulse, this gives a complete timing lock.

The width (active period) of the external V-pulse should be at least 1 line to guarantee that the camera starts in the correct field (See Figure 3).

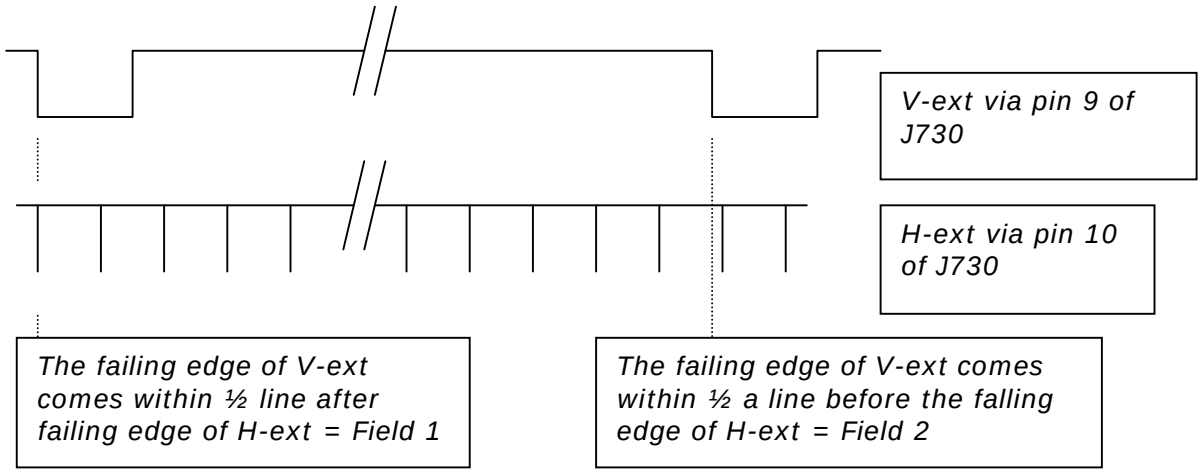


Figure 3. H & V lock

4.4. Line Lock

Line-lock means that a 50 or 60 Hz (PAL or NTSC) pulse is supplied to the camera (active low). The external V-pulse and the internal V-Pulse are compared with each other. The frequency (or phase) of the camera oscillator is adjusted via PLL until the two V-pulses are locked.
By feeding the external V-pulse (via pin 9 of connector J730) to the camera the camera is running in the line lock mode.

Allowing H-lock is important if the camera system always needs to be reset in the same field. By coupling the reset pulse to a H-pulse generator (connecting this also to the camera) the master is in full control when a reset occurs and in which field the reset occurs. Without the H lock this is not possible. Further there is no jitter of 32 microseconds (max).

4.5. Gain Control

4.5.1. AGC

The camera has an automatic gain control in the default mode. This function is responsible for the output signal remaining constant at a certain level. If the camera is pointed to a gamma reflection chart of 0.45 the output should be 1 Vp-p. This control circuit works with an integrator. This integrator generates from the video signal a signal that corresponds with the average value of the signal. This average is compared with an internal reference and depending on the outcome of the gain will increase or decrease.

4.5.2. Manual Gain Control

If the automatic gain control should be switched off, send via the I2C interface to command register 07h a value of 80h for fixed gain is 0dB. By sending FFh the gain goes to its maximum level. All values above 80h are fixed values. Below the gain control is automatic.

4.6. Gamma

The camera has a gamma function to correct the non-linear behavior of the CRT monitor. The gamma curve of the camera is 0.45. With this gamma setting the monitor is able to display the scene as we see it with our eyes.

However if the camera video signal is processed for pattern recognition this gamma function is often not wanted. To make this possible the 20/21D47X has a gamma option. This can be programmed via I^2C serial interface. Contact Videology for details. " This is like this because the 20D47X has no command function for gamma.

4.7. Back Light Compensation

The camera has a default setting of standard back light compensation (BLC) on. Backlight compensation serves to optimize the area of interest within the scene which is usually the central portion of the image. This means that for the electronic iris circuit only the central portion of the scene is taken into account to determine the level of the CCD output (see **Error! Reference source not found.**). When fixed shutter speeds are used this function has no effect.

Sometimes it can be required that the complete image should be used to determine the CCD output level. This function can be addressed via command register 03h.

The Back Light Compensation is fully programmable:
Size of the window and position of the window can be programmed. Also weighting factors (relation between the BLC window and rest of the image) can be programmed.

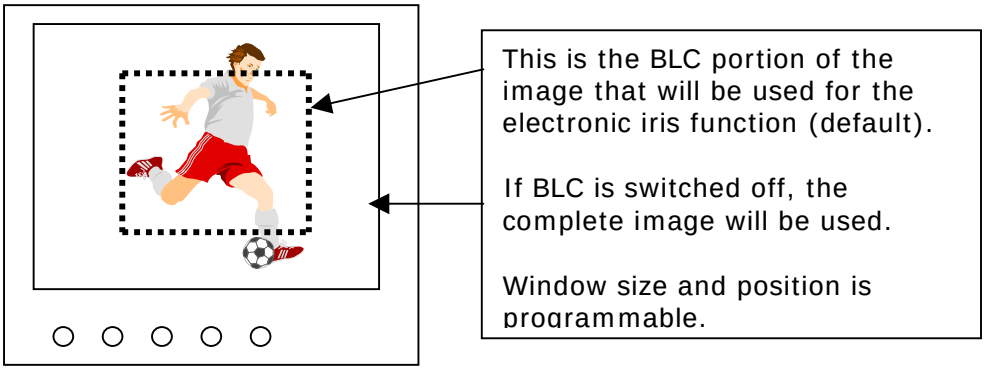


Figure 4. Back Light Compensation

4.8. Non-interlaced

The camera runs normally in the interlaced mode according to the PAL or NTSC standards.

This means that a full picture (frame) is built up out of two half pictures (fields) who are shifted half a line from each other. For a graphical view (see Figure 5).

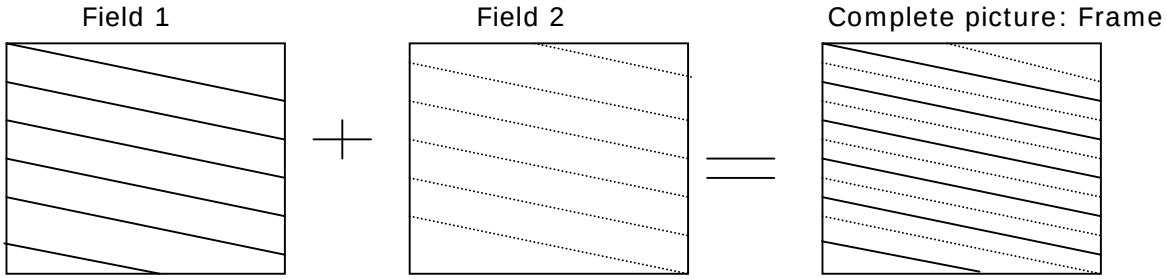


Figure 5. Interlaced Display

This means that every 40ms (for PAL) or 33.3ms (for NTSC) the camera has generated a complete picture.

However, sometimes the application does not require the high vertical resolution, but desires to have the same information each field (without the half line shift between the fields). In that case the two fields are identical to each other (See Figure 6).

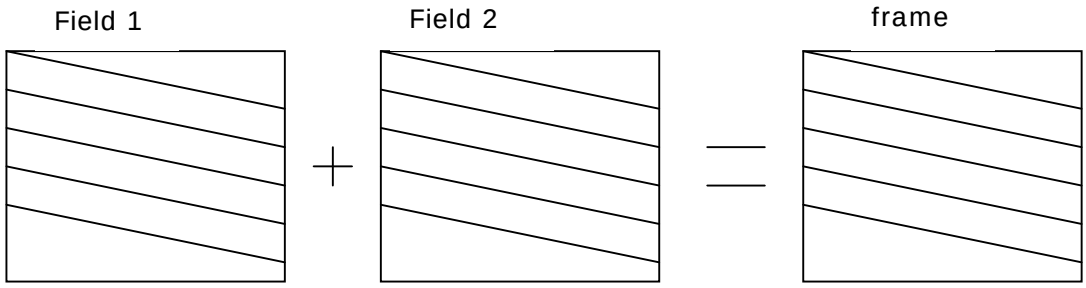


Figure 6. Non-Interlaced Display

In Figure 6 it can be seen that the vertical resolution is less compared with the interlaced mode (see Figure 5), but that the fields are identical to each other and therefore the frame rate is increased (doubled).

To put the camera in the non-interlaced mode send FFh to Command register 0Ah.

4.9. Frame Rate

The camera is normally working according to the NTSC or PAL standard. However, the components are selected in such a way that by increasing the main clock frequency the vertical frequency can be increased up to 75 Hz. To achieve this the new frequency of the crystal should become:

Camera	Vertical Frequency: 75 Hz
20D47X (NTSC)	35.79545 MHz
21D47X (PAL)	42.5625 MHz

Table 3. Crystal Frequencies

The crystal should be a standard type (fundamental).

4.10. Outputs

Via Software setting several output formats can be selected:

- CVBS standard output and Y/C (S-VHS)
- YUV analog output
- RGB analog output
- Also digital 8-bit YUV: 422 output is available (CCIR 656)

4.11. CPLD Flexibility

The CPLD can be programmed to perform extra functionality.
For instance: on request a camera can be made available with additional Low Vision features. The following functions can be programmed:

- B/W high contrast
- Magenta/black high contrast
- Green/black high contrast
- Yellow/blue comparator mode
- Amber/black high contrast
- Light blue/black high contrast
- Light magenta/black high contast

5. Software Control

5.1. Camera Software Protocol:

The camera has a serial control interface via three wires:

- Data wire
- Clock wire
- Ground wire

This interface operates similar as to the I^2C-protocol.

Data, address and registers are all 8 bit words. Graphical the interface is shown in Figure 7. The maximum speed limitation is 10kHz. The minimum speed should be higher then 100Hz. The write action to the EEPROM needs to be done with a waiting time between the write actions of at least 10msec.

Further a wait time is required between the commands, so that the internal communication has the time to do the required internal communication. The delay time between the commands should be at least 2msec.

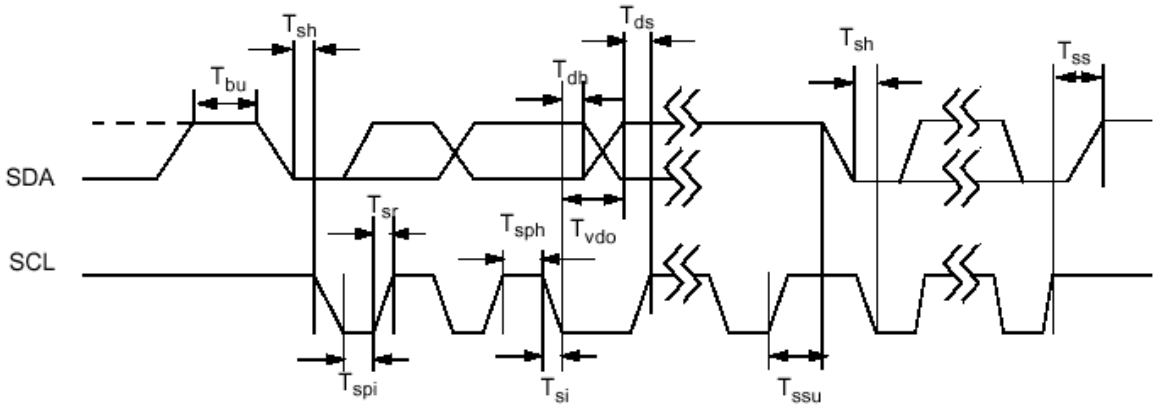


Figure 7. Communication timing

Standard I^2C address camera: 0x70
The communication-structure contains a Command block and a Data block.

Command block:
<START> <cam_address>ackn<acces_mode>ackn<device>ackn <register>ackn<STOP>

Cam_address	Acces_mode	device
Standard=0x70*	00=write to camera 01=read to camera 09=dump (write) EEPROM**	00=encoder 30=DSP 40=commands a0,a2,a4,a6= EEPROM

Data block (if acces_mode !=09, accesmode is not configured as dump-mode) :
<START><cam_addressR/W>ack<data>ackn/Nackn***<STOP>

Cam_address	Data:
Access mode=00: 0x70	Write data to camera with ackn
Access mode=01: 0x71	Read data from camera with NOT ackn.

*The address can be changed. In address 0xa0 of the EEPROM: 0xa2 is the address of camera stored. Camera can get new address if customer wants/needs!

**Special mode to access EEPROM faster for production. Block writing is not possible every time the camera address is required. First, both passwords have to be given before access is allowed!

***NOT acknowledge means: master send a clock low→high→low as with a normal acknowledge, but camera may not respond by pulling data line low. This must be checked otherwise the number of bits are not correct!

Example 1 write action:
Set white balance mode to Push to White, this means:

Command 40; register 00 and data 03:
Write action:
Command-block:
<start> 70 ackn 00 ackn 40 ackn 00 ackn <stop>
datablock:
<start> 70 ackn 03 ackn

description: camera-address 70, access mode write, device 40 (command), register 00, datablock: write address 70 , data 03.

Example 2 read action:
Command 40; register 00 and read data :
Read action:
Command-block:
<start> 70 ackn 01 ackn 40 ackn 00 ackn <stop>
datablock:
<start> 71 ackn data (returned) Nackn

description: camera-address 70, access mode read, device 40 (command), register 00, datablock: read address 71 , camera will sent data.

5.2. Camera Configuration:

The device addresses have two values, one for read the other one for write. The difference is that the last bit (LSB) is set to one. For the communication the next device addresses are available:

Device	Device write	Device read
DSP	0x30	Not possible
Commands	0x40	0x41
EEPROM page 1	0xa0	0xa1
EEPROM page 2	0xa2	0xa3
EEPROM page 3	0xa4	0xa5
EEPROM page 4	0xa6	0xa7

Table 4. Device addresses

It is not possible to read from the DSP. The DSP is a write only device.

Don't write to the DSP because it can make the camera non-functional.

EEPROM pages 3 and 4 are protected by a password! The normal user may not have access to these two pages since the back up settings and production date is saved in here.

The DSP settings are directly mapped on EEPROM page 1.

The camera will recognize several commands. Often these will be a combination of several internal commands to fulfill a certain task. To send commands to the camera, first the device number 0x40 has to be send. After that, the command self (at the normal place, the address will be found) must be send, and the data third.

5.3. I^2C Address

The camera has an I^2C address so that more than one camera can be connected to I^2C bus.

The camera default address is 0x70. In case user might have forgotten the new address, he can reset it back to the factory default by connecting pin 16 of the microprocessor (port 0.5, test-point available on board) to ground:

Connect to ground for at least 4 seconds.

The I^2C address is stored in the EEPROM page 2 address 0x90 (hex).

To change this address one should write: device 0xa2; address 0x90; value 0xXX.

XX is free to choose. With this method you can have 256 different I^2C addresses for the camera.

With device 0xa3 one can read the value.

5.4. Communication Reset

Sometimes it can happen that communication is halted. The u-processor then will reset the communication lines.

5.5. Command Registers

To address the command 40h has to be send. Direct after that the command register and value.

The following commands can be executed.

For more detail please see the readme.doc which is with the SW-package.

Command	Command number	Data range
White balance mode	0x00	0x00: auto white balance 0x01: fixed white balance mode 1 0x02: fixed white balance mode 2 0x03: push to white
Output Mode	0x01	0x03: CVBS &Y/C output mode 0x01: RGB output mode 0x00: YUV output mode
Reserved	0x02	Optional Features (for instance Low-Vision modes).
Back light comp.	0x03	0x00: BLC on 0xff: BLC off
RESET: load defaults	0x04	0xac: reset load default values
Mirror mode	0x05	0x00=normal, 0xff=mirror
Shutter mode	0x06	0x00: electronic iris 0x01: 1/50 or 1/60 sec 0x02: flickerless 0x03: 1/250 0x04: 1/500 0x05: 1/1000 0x06: 1/2000 0x07: 1/10000 0x08: 1/20000 0x09: 1/50000 0x0a: 1/100000 0x0b: 1/25 or 1/30 sec (intermittent frame readout) 0x0c: 1/12.5 or 1/15 sec (intermittent frame readout) 0x0d: 1/6.5 or 1/7.5 sec (intermittent frame readout) 0xff: hardware control 8 values, via PROG-MODE pins connector J710.
Gain control	0x07	0x00: auto mode 0x80: fixed gain minimal 7 LSB's are fixed gain: The MSB indicates fixed gain 0xff: fixed gain maximal gain
Non-interlaced	0x0a	0x00: interlaced 0x0f: non-interlaced 0xff: hardware control via PROG-MODE 4 (J710)
Edge enhancement	0x0b	0xc0 edge enhancement off gain range 0x00 upto 0x1F
Standby	0x0c	0x00 : DSP active, 0xff : DSP standby after a power down and up the camera will start , does not stay in standby.

BLC window can be programmed for special light situations:

Size BLC window	0x08	64 windows can be defined over the whole active pixels. This means that for PAL: H = 94 pixels and V = 72 pixels ; For NTSC: H= 96 pixels and V = 62 pixels. Size H x V 0x00 1H x 1V 0x01 1H x 2V 0x02 1H x 4V 0x03 1H x 8V 0x04 2H x 1V 0x05 2H x 2V 0x06 2H x 4V 0x07 2H x 8V 0x08 4H x 1V 0x09 4H x 2V 0x0A 4H x 4V 0x0B 4H x 8V 0x0C 8H x 1V 0x0D 8H x 2V 0x0E 8H x 4V
Position BLC window (9 window positions possible)	0x09 (See also figure below)	0x00 center 0x01 Top left 0x02 Top center 0x03 Top right 0x04 Center left 0x05 Center right 0x06 Bottom left 0x07 Bottom center 0x08 Bottom right

1	2	3
4	0	5
6	7	8

Figure 8. BLC position

The BLC weighting factor can also be programmed. The value of this factor (which in fact is a number which determines how the ratio between window and the rest of the image is calculated) is stored in EEPROM, see (table below).

The command setting is stored in side the memory of the camera. After a power down the camera will come up with the last used settings again (except standby).

5.6. EEPROM Special Settings

The fixed white balance settings are programmed in EEPROM.

These values can be altered.

Address in EEPROM page 0xA2/A3	Content
0x91	Fixed white balance mode 1 BLUE
0x92	Fixed white balance mode 1 RED
0x93	Fixed white balance mode 2 BLUE
0x94	Fixed white balance mode 2 RED
0x95	Fixed white balance mode 3 BLUE
0x96	Fixed white balance mode 3 RED
0x97	Push to White correction factor
0x98	BLC weighting factor
In case of encased cameras (see note):	
0xEF	Feature register: 00 is software command control FF is dipswitch command control

Note: Videology Imaging Solutions encased camera model number is 20/21D779.

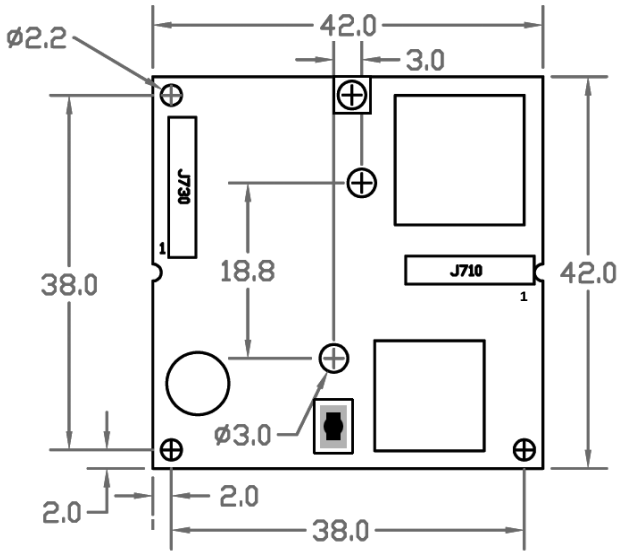
With this camera dipswitch command control is enabled (see instruction manual 20/21D779). This means that I^2C commands are not accepted. You can read the command status and you read and write to the DSP and EEPROM registers. When you want to control the commands via I2C you have set the Feature Register.

6. Mechanics/Connectors

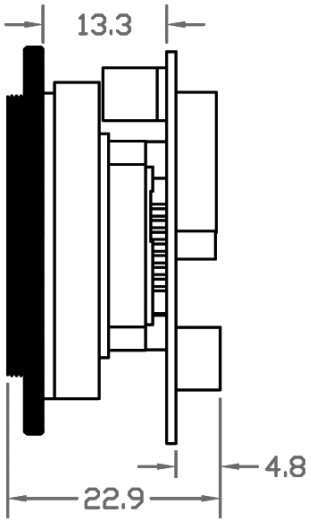
This chapter gives the mechanical information about the 20/21D47X. This mechanical information also includes connector information.

6.1. Board Mechanical Dimensions

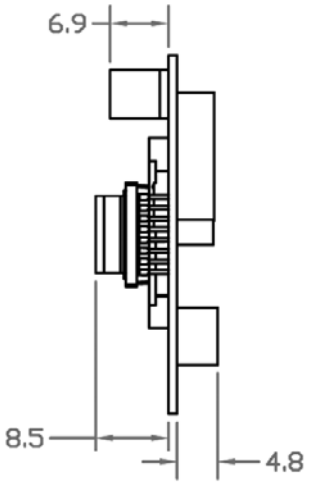
Back of Camera



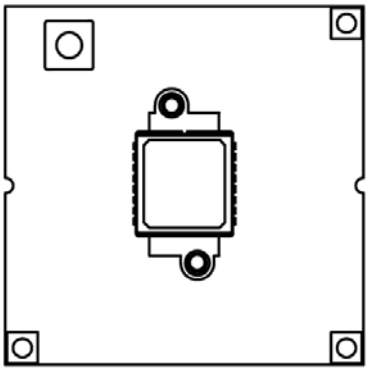
Camera with CS Mount



Camera without CS Mount



Front of Camera



6.2. Connectors

The camera has one connector that can be used as interfaces for the user of the camera. Both are located at the backside of the camera (see Figure 9).

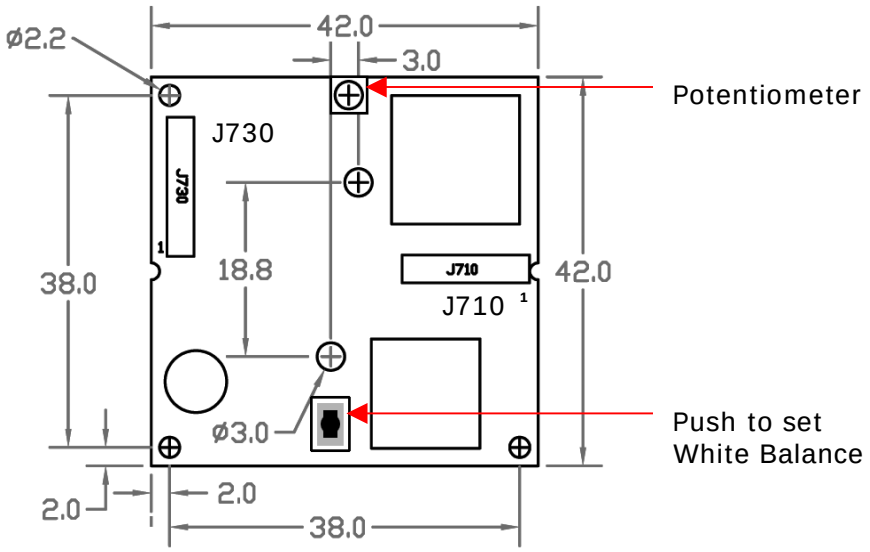


Figure 9. Connectors

J730 is a 13-pole JST connector, type BM13B. J710 is a 24 pole JST flat foil connector, type 24FLT-SM1-TB. Pin connection:

Pin no.	Pin function J730			Pin no.	Pin function J710 flat foil connector
1	Horizontal Sync out			1	Ground
2	GND			2	SCLOCK I2C
3	+12V IN			3	SDATA I2C
4	PWB (push to white)			4	MODE3-LV
5	GND			5	MODE2-LV
6	Y (lum)	G	Y	6	MODE1-LV
7	CVBS	B	U	7	MODE0-LV
8	C (Chr)	R	V	8	Pixel Clock
9	VEXT (vertical sync in)			9	Ground
10	HEXT (horizontal sync in)			10	PROG-MODE4
11	Vertical Sync out			11	YUV-out-7 msb-bit digital out
12	SDATA I2C			12	YUV-out-6
13	SCLOCK I2C (black wire)			13	YUV-out-5
				14	YUV-out-4
				15	YUV-out-3
				16	YUV-out-2
				17	YUV-out-1
				18	YUV-out-0 lsb-bit digital out
				19	Ground
				20	V-SYNC out
				21	PROG-MODE2
				22	PROG-MODE3
				23	H-SYNC out
				24	PROG-MODE1

Please note: connector J710 has been changed with respect to previous models!

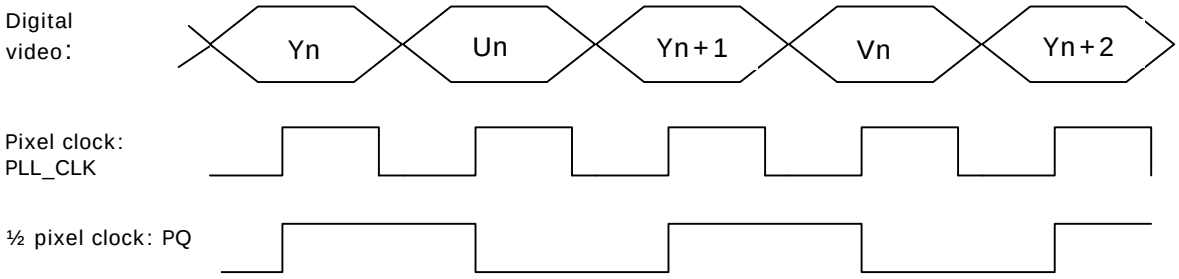
7. Specifications

Electronic		**20D476/ 479 NTSC**	**21D476/ 479 PAL**
Image Sensor		1/3" IL	
Active Pixels (HxV)		768 x 492	752 x 582
Resolution		470 TVL	
Horizontal Resolution		470 (TVL) CVBS, 490 (TVL) YC (SVHS)	
Sensitivity		<0.5 Lux (50 IRE) F1.2 Lens transmission 80%, scene reflection 75%	
Signal to Noise Ratio		> 48 dB (AGC off)	
Gamma		Default 0.45, 1.0 Selectable via software	
Gain		Automatic (26 dB default) Manual / Fixed via software	
Synchronization		Internal (X-tal coupled), H&V lock, line lock	
Back Light Compensation		Selectable via software	
White Balance		Automatic (default) 3 Fixed modes via software Push to set via hardware or software	
Shutter Speed		Automatic from 1/50 to 1/100,000	Automatic from 1/60 to 1/100,000
		8 Fixed speeds via hardware 11 Speeds via software	
Scan Mode		Interlaced / Non-interlaced 75Hz option, specific model	
Flickerless Mode		1/100 sec	1/120 sec
Contour Enhancement		Selectable Horizontal and vertical via software	
Mirror Mode		On/Off Selectable via software	
Iris		CCD Iris default, video iris DC Iris output via option board 60PB24VDL	
Video Output	Analog	1Vp-p video 75 ohms composite optional: Y/C (SVHS), RGB	
	Digital	YUV 8 bit	
Power Supply		8~16VDC, 12VDC Nominal	
Power Consumption		<2.0W excluding: auto iris power consumption	
Environmental			
Operating Temperature		-15° C ~ 55° C (5° F ~ 131° F)	
Storage Temperature		-25° C ~ 70° C (-13° F ~ 158° F)	
Mechanical			
Dimensions W x H x D		42mm x 42mm x 17mm (1.65" x 1.65" x 0.66")	
Lens Mount	20/21D476	Metal M-12 board lens mount with reference plate, 12mm diameter, 0.5mm pitch	
	20D479	Metal CS mount with reference plate	
	60VZZ0030	Optional C mount with interface ring	
Interfaces	Analog	13 Pole AMP	
	Digital	24 Pole Flex foil connector	
Power Supplies	60PR12DC500	12VDC	
Cables (Included)	60C1011	13-pin with flying leads	
Software			
SFT-03001		Software control program available	

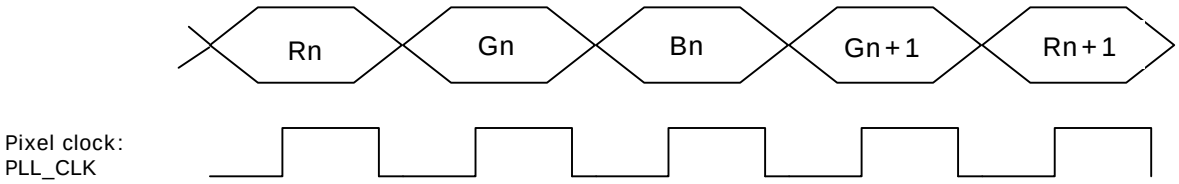
8. Digital Output Format

8.1. YUV Output

The output bus is 8 bits wide. This means YUV are multiplexed according to the following sequence:



8.2. RGB Output



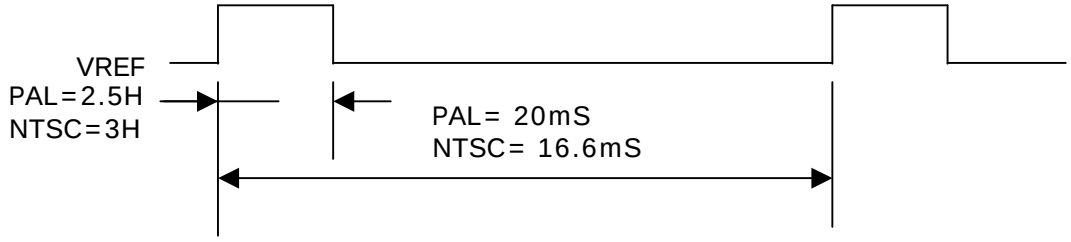
The PLL_CLK clock rate is:

PAL:	28.375Mhz (Field rate 50Hz)
NTSC:	28.63632Mhz (Field rate 60Hz)

Beside these pixel related signals on the output connector there is also a HREF signal available as sign of the Horizontal active video period. The polarity of this signal is programmable.

Below is the Horizontal pulse (equal to active pixel data) one must set register 0x03 of DSP to value 0x58 to obtain this (active low) pulse. In normal mode (H = active high) it is programmed to 0x38 (this is mostly used for H-and V-lock).

In vertical direction a VREF signal is available. This signal has a positive polarity. The signal is present during the vertical serration pulses.



9. Contact Information

For technical assistance with this product, please contact the supplier from whom the product was purchased.

For OEM inquiries, contact Videology Imaging Solutions:

North / South America:	**Europe:**
Videology Imaging Solutions Inc. 37M Lark Industrial Parkway Greenville, RI 02828 USA Tel: (401) 949-5332 Fax: (401) 949-5276	Videology Imaging Solutions Europe Neutronenlaan 4 NL-5405 NH Uden, Netherlands Tel: +31 (0) 413 256 261 Fax: +31 (0) 413 251 712

Please visit our WEB-site at: http://www.videologyinc.com/

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