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Application Note

24B5.0xUSB3/
24B5.0xDIG
Preliminary

24B5.0XUSB3 shown

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1. Document History

Revision	Issue Date	Reason	CN#
Rev 0.1	15-Nov-2015	Initial release	-
Rev 0.2	18-Nov-2015	Drawings and images added	-
Rev 0.3	19-Aug-2016	Update according to design (Preliminary version)	-
Rev 0.4	14-Nov-2016	Update for final design changes	-
Rev A	17-Feb-2017	Released for public dissemination	-

2. Introduction

The 24B5.0x is a UVC compliant, 5 megapixel, Black and White, USB 3.0 camera designed around a 1/2.5" Format CMOS sensor.

The camera outputs 14.5 fps at the maximum resolution of 5MP (2592 x 1944). Higher frame rates are available at lower resolutions. Binning and row/column skipping modes are supported at a resolution of 720P and 640 x 480.A total of 8 GPIO lines are available, and these can be configured to suite customer requirements.

The camera is available in two configurations, the 24B5.0x-DIG and the 24B5.0x-USB.
Both models provide a 10 bit parallel digital output, and the USB model provides an additional 8-bit USB 3.0 compliant output.

Both camera models are available with either M12 or CS lens mounts.

3. Specification

3.1 Electrical

	24B5.0x-DIG	24B5.0xUSB3
Image sensor	CMOS 1/2.5" 5MP	
Recording Pixels	2592 x 1944	
Pixel / image size	2.2µm x 2.2µm	
Scanning system	Progressive	
Shutter type	Electronic rolling, automatic/fixed	
Resolution / Frame rate	5MP (2592 x 1955) 14.5/12.5 fps 1080P 30/25 fps 720P 60/50 fps VGA 120/100 fps	
Pixel clock rate	74.25MHz	
Sensitivity	Normal mode: 1.0 Lux Digital slow shutter: 0.3 Lux	
Signal to Noise ratio	>38dB	
AGC	Automatic/manual	
Synchronization	Internal	
Shutter type	Electronic rolling, automatic/fixed	
Mirror/flip	Horizontal & Vertical On/Off	
Video output	Digital: Y out (10-bits @ 74.25MHz)	Digital: Y out (10-bits @ 74.25MHz) USB3.0 output: 8 bits
Supplied Voltage	+4.5 – 5.0V	
Current drawn	<250mA (@ 5V)	<350mA @5V
Power consumption	1.3Watt	1.8Watt
Communication	I^2C	
Dynamic range	70.1dB linear	

Environmental		
Operating Temp.	-15° ~ 60° Celsius (14°F ~ 131°F)	
Operating Humidity	20% ~ 90% RH	
Storage Temp.	-40° ~ 80° Celsius (-22°F ~ 176°F)	
Storage Humidity	94% RH	

Mechanical		
Dimensions WxHxD (mm)	32 x 32 x 15 (no lens mount)	32 x 32 x 20 (no lens mount)
Weight	40 Grams	40 Grams
Lens mount	Replace x in type number: 5: M12 lens mount 7: no lens mount 8: CS lens mount	
Connectors	Backside: Digital output 30-pin;*30P4.0-JMCS-G-8-TF* GPIO interface 8 pins:JST	Backside: Digital output 30-pin;*30P4.0-JMCS-G-8-TF* USB 3.0 connector type GPIO interface 8 pins: JST

3.2 Mechanical

The camera is a double board design with overall dimensions as shown in Figure 1.

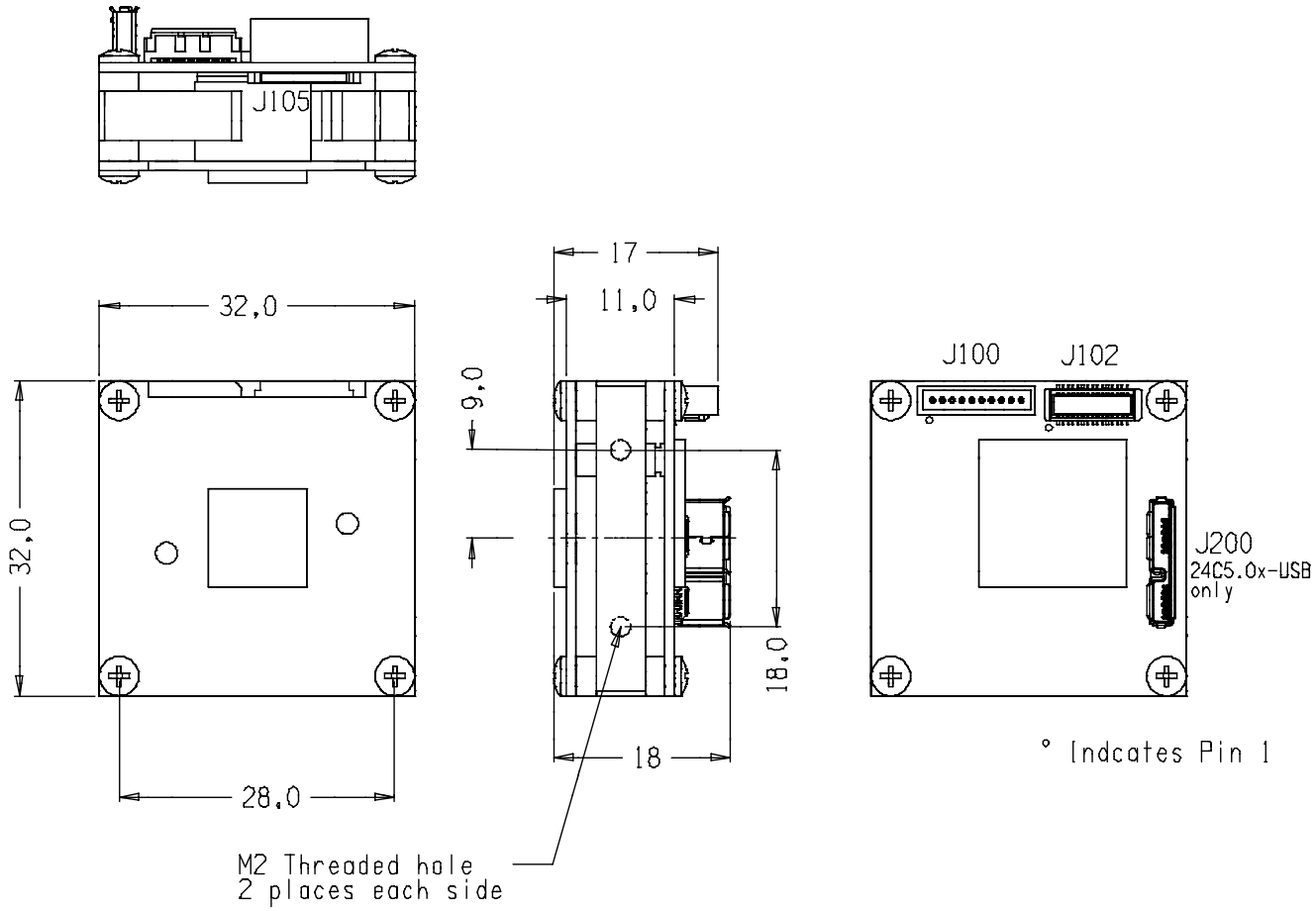


Figure 1. Camera Dimensions (no Lens Mount)

3.3 Connectors

3.3.1 Digital Video Output (DIG and USB Versions)

J102 – Molex- 501920			
Pin #	**Pin name**	**Pin #**	**Function**
1	Gnd	2	Gnd
3	Y0	4	IO-TBD
5	Y1	6	IO-TBD
7	Y2	8	IO-TBD
9	Y3	10	IO-TBD
11	Y4	12	IO-TBD
13	Y5	14	IO-TBD
15	Y6	16	IO-TBD
17	Y7	18	IO-TBD
19	CLOCK	20	IO-TBD
21	HREF	22	Gnd
23	LV	24	VREF
25	Y8	26	IO-TBD
27	I2C-SDA	28	I2C-SCL
29	Y9	30	+5V

3.3.2 GPIO/ Power

J100 – JST-SM10B-SRSS	
Pin #	**Function**
1	GPIO0(SNAP USB3)
2	GPIO1
3	GPIO2
4	GPIO3
5	GPIO4
6	GPIO5
7	GPIO6
8	GPIO7
9	GnD
10	Vin (4.5 – 5)

3.4 Lens mount options

Both camera models area available with either an M12 or CS lens mount.
Table 1 below gives the part number for each configuration.

Table 1. Lens Mount Options

Lens interface	Camera type number	
	USB3 version	DIG version
No lens mount	24B5.07USB3	24B5.07DIG
M12 lens mount	24B5.05USB3	24B5.05DIG
CS-lens mount	24B5.08USB3	24B5.08DIG

The overall dimensions of camera with M12c and CS mounts are shown in fig 2 and 3 below.

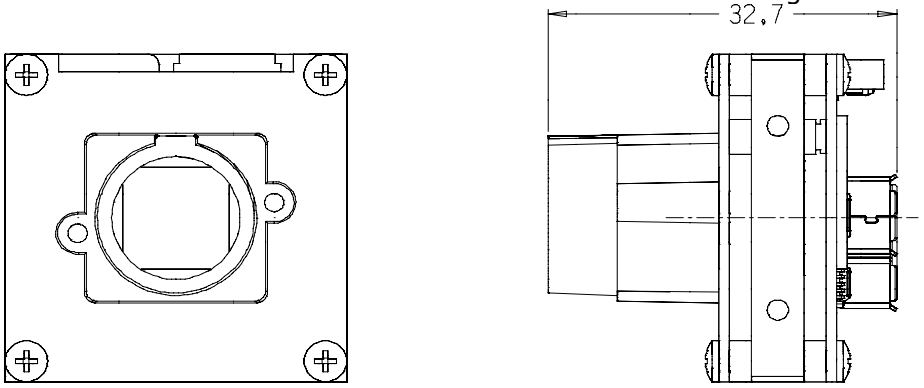


Figure 2. Camera with M12 Lens Mount

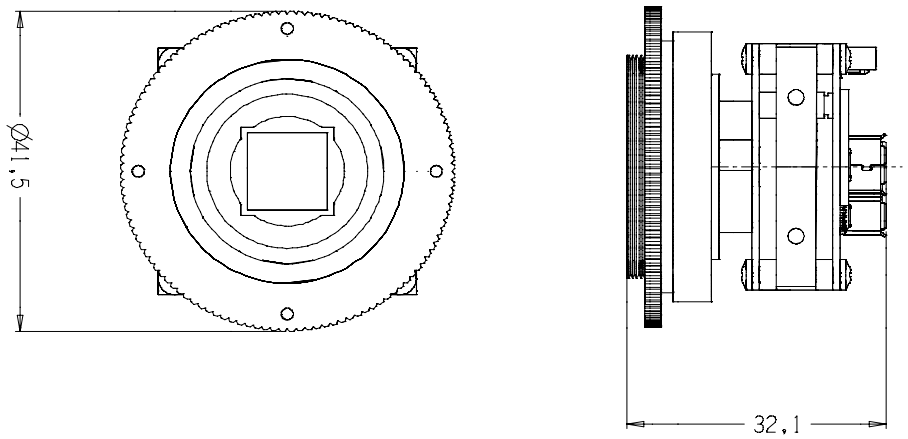
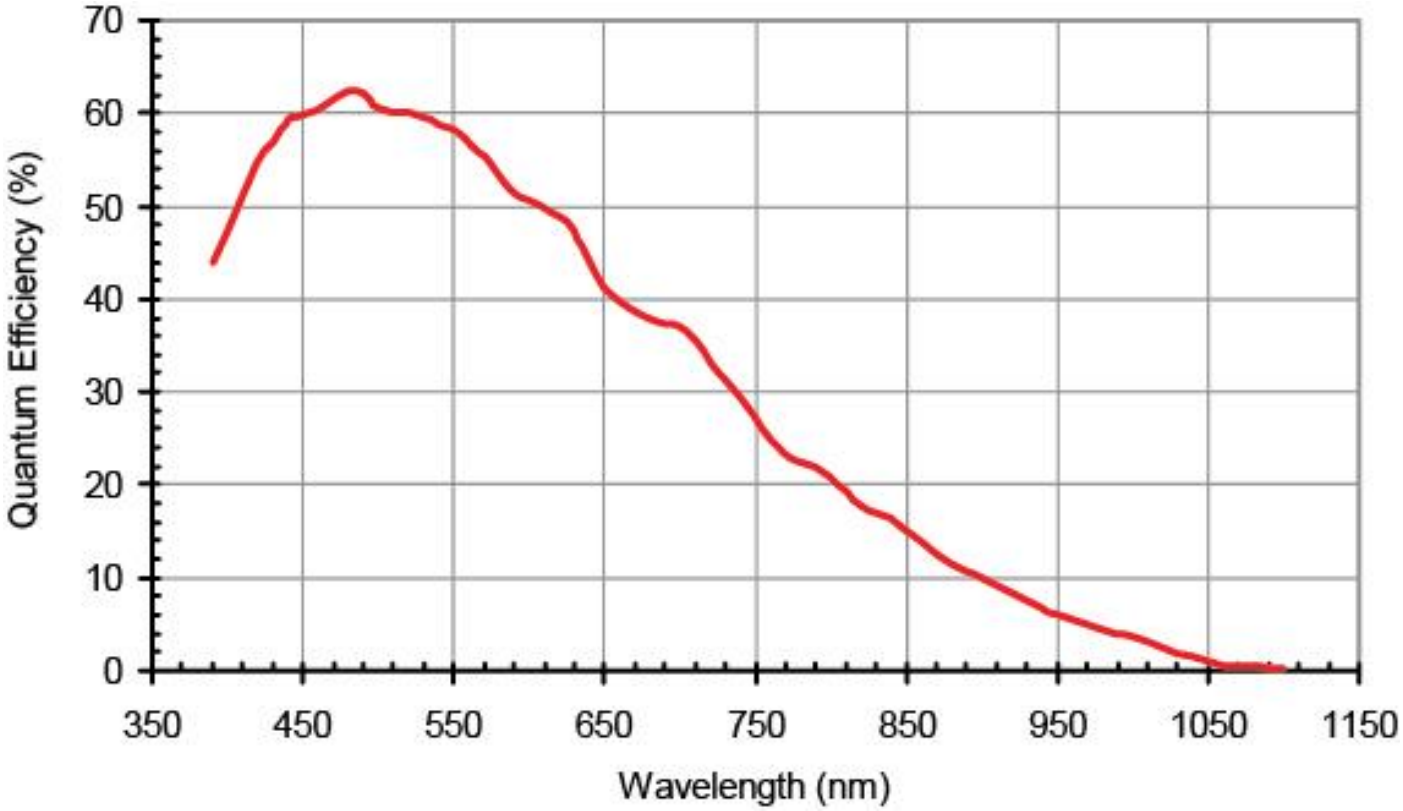


Figure 3. Camera with CS Mount

3.5 Spectral Response



4. Digital output

The camera has a 10 bit parallel digital output with separate horizontal and vertical timing signals LV and HV.

Figure 4 shows the timing diagram for the data clock and H and V pulses.

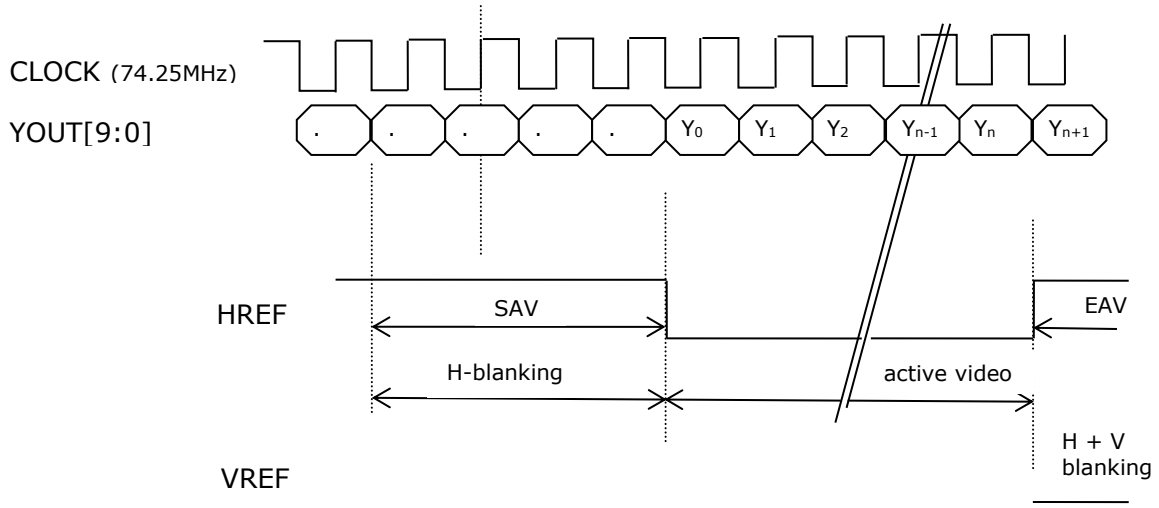


Figure 4. Digital Output Timing

4.1 Output formats

The camera supports a range of standard formats as shown in Table 2.

Table 2. Standard formats supported

HD mode	Sub sampling Mode	Frame rate [Hz]	Resolution HxV	Active pixels size HxV	Line freq. [KHz]	Pixel clock [MHz]
Full res	N/A	14.5	2592x1944		28.51	74.25
Full res	N/A	12.5	2592x1944		28.31	
1080P	N/A	30	1920x1080	2640x1125	35.06	74.25
1080P	N/A	25	1920x1080	2200x1125	34.76	
720P	N/A	60	1280x720	1980x750	45.04	74.25
720P	N/A	50	1280x720	1650x750	37.52	
720P	skipping/binning	55	1280x720	2560x1440	40.77	74.25
720P	skipping/binning	50	1280x720	2560x1440	36.50	
VGA	N/A	120	640x480		61.18	74.25
VGA	N/A	100	640x480		51.08	
VGA	skipping/binning	60	640x480	2560x1920	30.67	74.25
VGA	skipping/binning	50	640x480	2560x1920	25.55	

5. I²C Camera Communications

The camera uses a 2 wire serial (I2C) communication interface for control and configuration.
This serial bus consists of a line for the clock signal (I2C-SCL), a line for the data signal (I2C-SDA), and a line for ground. The camera will act as a slave device on this bus.
The protocol supports clock speeds from 1 kHz – 100 kHz.

The camera address is 0x70/0x71.

The communication protocol consists of two blocks. The first block is a command block, followed by the data block.

The command block is always 4 bytes long. It contains the camera address (write only = 0x70), a mode byte, device address and register address.

The Data block is either read or write, depending upon the camera address used. An address of 0x70 denotes a write command, an address of 0x71 denotes a read command.
Similarly, the mode byte of the command block also indicates a read or write. This is indicated with the least significant bit: a 0 indicates a write action and a 1 a read action.

5.1 Timing

Note: there is a minimum delay time (delay1) required between the command and data block. This delay depends on the direction of communication (write or read). Additionally, there is a minimum delay time (delay2) between a data block and the next command block.

Command block	Delay1	**Data block**	Delay2	**Command block**	Delay1	**Data block**

Table 3 below gives the minimum values for delay1 and delay2 for the various read and write operations.

Table 3. Minimum value of delay1 between command and data bytes:

Type of communication	**Minimum Delay (ms)**	
	Delay1	Delay2
Read from command register followed by another read	5	1
Write to command register followed by another write	1	80
Read from command register followed by a write to the EEPROM	5	1
Read from EEPROM followed by write to EEPROM	80	5
Write to DSP followed by a write to another device	1	80

5.2 The command block

Each command block consists of 4 bytes, as shown below:

Command block									
	Byte 1		Byte 2		Byte 3		Byte 4		
start	Cam addr W	A	Mode byte r/w	A	Dev add	A	Reg addr	A	Stop

A= acknowledge

- The 1st byte is the camera address. The only valid value is the camera write address, default 0x70
- The 2nd byte is the mode byte. The mode byte tells the camera the host wants to read or write to the camera. If the host wants to read the LS-bit is 1.
- The 3rd byte is the device address inside the camera.

Valid values for the mode byte and device address can be found in the table below:

Mode value (2nd byte)	Device address	description
0x52/0x53	0x30/0x31	Command access
	0x38/0x39	FPGA access
	0xa0/0xa1	EEPROM 1st page
	0xa2/0xa3	EEPROM 2nd page
	0xa4/0xa5	EEPROM 3rd page
	0xa6/0xa7	EEPROM 4th page
	0x1C/0x1D 0x46/0x47	Opt AF driver DRV201 Opt AF driver HV892
	0xBA/0xBB	Device address 0xBA/BB is the Sensor. In this case the data consist of bytes either for read or write.

- 4TH byte is the register address. This byte can have any value between 0x00 and 0xff.

5.3 The Data block

This block is generally 2 bytes. The difference here is that the camera can either send or receive data via this block.

The format for each type of operation is shown below.

Data block: data sent from Host to camera					
	Byte 1		Byte 2		
start	Cam addr W	A	data	A	stop

A= acknowledge

Data block: data sent from Camera to Host					
	Byte 1		Byte 2		
start	Cam addr R	A	data	NA	stop

NA= Not acknowledge

The first byte is either the camera write or read address. The default camera write address is 0x70, and the default read address is 0x71.

In order to send or receive two data bytes to the sensor, the device address 0xBA or 0xBB is used.

In this case the structure of the command block will be as shown below:

Data block: data from host to camera							
	Byte 1		Byte 2		Byte 3		
start	Cam addr W	A	Data byte MSB	A	Data byte LSB	A	stop

A= acknowledge

Data block: data from Camera to host							
	Byte 1		Byte 2		Byte 3		
start	Cam addr R	A	Data byte MSB	A	Data byte LSB	NA	stop

A= acknowledge, NA = not acknowledge

- The first byte is either the camera write or read address. The default camera write address is 0x70, and the default read address is 0x71.

6. I²C Command registers

The camera has several user accessible command registers (mode byte is 0x52/0x53 and device address 0x30/0x31) which can be used to configure and control the camera behavior. These registers can be used to control exposure and gain control modes, image display settings, backlight and auto focus parameters etc.

A detailed description of each of the control registers is given in section 8.

In order to maintain the camera settings and configuration upon power cycling, the register settings are stored in an EEPROM. The EEPROM contents and addresses are given in Table 4

Table 4. EEPROM page addresses and contents

EEPROM Page	Device Addr. W/R	Contents
0	0xa0/0xa1	Startup command register settings
1	0xa2/0xa3	FPGA /Video processing default settings
3	0xa4/0xa5	Factory default command register settings.
4	0xa6/0xa7	Default sensor Register settings

It is not recommended for the user to change the registers in page 1, 2 or 3 of the EEPROM.. Therefore these registers are write protected.
This document only describes the command registers and EEPROM mapping.

6.1 Register Overview

Device Address(w/r)	Register Address	Function
		Camera
0x30/0x31	0x00	AEX control mode1
0x30/0x31	0x01	Resolution mode
0x30/0x31	0x02	AEX control mode 2
0x30/0x31	0x03	Fixed gain value (gain manual mode)
0x30/0x31	0x04	AEX reference level
0x30/0x31	0x05	Image orientation (mirror / flip)
0x30/0x31	0x06	Edge enhancement mode
0x30/0x31	0x07	Edge enhancement gain
0x30/0x31	0x08	Edge enhancement AGC start suppression point
0x30/0x31	0x09	Edge enhancement AGC end suppression point
0x30/0x31	0x0B	AEX reference hysteresis.
0x30/0x31	0x0C	AGC maximum gain.
0x30/0x31	0x0D	Contrast Level
0x30/0x31	0x10	BLC mode
0x30/0x31	0x11	BLC gain/weight factor
0x30/0x31	0x12	Fixed shutter speed fine control value
0x30/0x31	0x13	BLC window size
0x30/0x31	0x14	BLC window position
0x30/0x31	0x15	Brightness control
0x30/0x31	0x16	Output mode USB (optional data reduction)
0x30/0x31	0x17	Gamma correction
0x30/0x31	0x18	2D Noise Reduction mode
0x30/0x31	0x19	2D Noise Reduction gain
0x30/0x31	0x1A	2D Noise Reduction start point
0x30/0x31	0x1B	2D Noise Reduction end point
0x30/0x31	0x50	EEPROM Register save/restore command
0x30/0x31	0x70~0x77	Bayer pattern compensation registers
0x30/0x31	0xF6	Camera model (read only)
0x30/0x31	0xFC	Set Password (MSB) (write only)
0x30/0x31	0xFD	Set Password (LSB) (write only)
0x30/0x31	0xFF	Software revision number (read only)

7. Detailed register information

The following chapters describe each function and associated register(s) in more detail.

7.1 AEX control mode

The camera supports four basic exposure control modes which can be selected via register 0x00 bits [1:0] as shown in Table 5.

Table 5. Auto Exposure/Gain control modes

Reg 0x00 bits[1:0]	Mode
00	Auto Shutter and Auto Gain
01	Fixed Shutter Auto gain
10	Auto Shutter and Fixed Gain
11	Fixed Auto Shutter and Fixed Gain

7.1.1.1 Full auto mode

In full auto mode, the camera will automatically adjust the shutter speed (integration time) and gain value to maintain a constant output level.

In this mode, register 0x04 serves as a reference level. The output level of the camera can be increased or decreased by raising or lowering the reference level.

When the scene illumination level is high, the output level is controlled predominantly by the shutter speed. When the scene illumination is low, the gain control is used predominantly to maintain the output level.

The operation in illustrated in Figure 5.

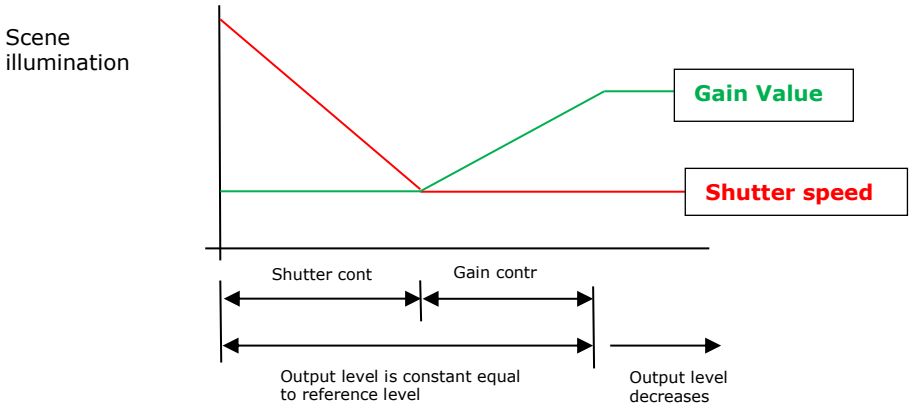


Figure 5. Automatic exposure/Gain control

To prevent the camera from constantly adjusting to minor variation in the illumination level, there is a certain level of hysteresis in the control loop. As long as the signal level stays within the range defined by the hysteresis, the shutter and gain controls will remain unchanged, as shown in Figure 6. The hysteresis is adjustable by the user via register 0x0B. This register sets both the low- and high hysteresis levels as a percentage of the reference level.
Example: When the AEX Reference level register 0x04 is set to 0x60 =(96 in decimal) and the AEX Hysteresis register 0x0B is set to 0x10 (=16 in decimal), the real hysteresis value is 16 / 100 x 96 = 15 and so the low and high thresholds are set to 96 ± 15.

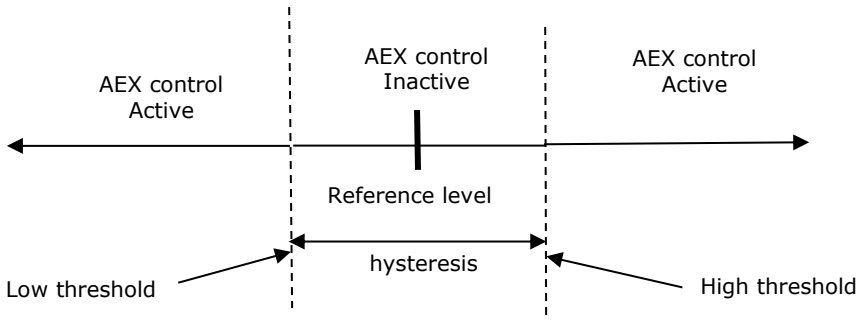


Figure 6. Auto Exposure Hysteresis

#define GAIN_START_DELAY 3 // number of frames that an image is beyond the aex reference band before aex control will start.

#define GAIN_STOP_DELAY 2 // number of frames that an image should be within aex reference band before aex control will stop/

7.1.1.2 Fixed shutter Mode

In this mode, the camera shutter speed can be set in conjunction with either a fixed or automatic gain option as defined in Table 5.

There are two fixed shutter modes, one providing a range of preset fixed shutter speeds and the other providing a finer level of speed control.

In the first option there are 8 predefined shutter speeds selectable via bits [6:4] of register 0x00. Note that bit [0] must be set to 1 and bit [7] of register 0x02 must be 0.
The fixed shutter speeds are given in Table 6

Table 6. Preset Fixed Shutter speeds

Reg 0x00 Bits[6:4]	Shutter period (Integration time)
000	Full Frame Period
001	7/8 X Full Frame Period
010	6/8 X Full Frame Period
011	5/8 X Full Frame Period
100	4/8 X Full Frame Period
101	3/8 X Full Frame Period
110	2/8 X Full Frame Period
111	1/8 X Full Frame Period

In the second mode, the shutter speed can be set in much finer steps.
To access this mode bit [0] must be set to 1 and bit [7] in register 0x02 must be 1.

Via register 0x12 the shutter speed can be set in fine steps, for which each step is a 1/256 part of the maximum shutter speed. This means that a value of ***m*** results in a fraction equal to (m + 1)/256 of the maximum shutter speed (for example, if the value is 0x7F, the shutter speed is half of the maximum shutter speed).

Note that the maximum shutter speed depends on the resolution setting; for full 5Mp resolution it is 1943 lines for VGA it is only 479 lines.

7.1.1.3 Manual (fixed) gain Control

As with the shutter speed, the gain can be set to a fixed value in combination with a fixed or automatic shutter.

To put the camera in a manual gain mode, bit [1] of register 0x00 must be set to 1.
The gain value is then set via register 0x03 as shown in Table 7.

Reg 0x03 value		Analog Gain Multiplier	Digital Gain Multiplier	Total Gain
hex	dec			
0x00	0	1.00 x	1 x	1.00
0x01	1	1.25 x	1 x	1.25
0x02	2	1.50 x	1 x	1.50
0x03	3	1.75 x	1 x	1.75
0x04	4	2.00 x	1 x	2.00
etc				
0x39	57	15.25 x	1 x	15.25
0x3A (analog max)	58	15.50 x	1 x	15.50
0x3B	59	15.50 x	9/8 x	17.50
0x3C	60	15.50 x	10/8 x	19.38
etc.				
0xB1	177	15.50 x	127/8 x	246.06
0xB2 (=max)	178	15.50 x	128/8 x	248.00

Table 7. Fixed Gain settings

The formula used for calculating the total gain (with the register value as input) is as follows:
if (*value* ≤ 58) then
    total gain = (4+*value*)/4 // This is the analog domain
else
    total_gain = 15.5*(1+*value*-58)/8 // This is the digital domain

7.1.1.4 AEX control speed

The speed of the auto exposure control loop can be set via bits[6:4] of command register 0x02 .
The AEX control speed value represents a time constant for both the shutter and gain control loops. A value of 0 sets the time constant to a minimum of 400 milliseconds, which gives the fastest response. Each increment of the speed value adds 400 milliseconds. So the maximum value of 7 provides a time constant of 2.2 seconds (400ms + 7 * 400ms), which is the slowest response.

7.1.2 Resolution mode

The camera supports a range of standard HD resolution display modes.
By reducing the resolution, the frame rate can be increased or the total data can be reduced.

The resolution is set via bits[5:4] of command register 0x01 as shown in Table 8

Table 8. Screen Resolution settings

Reg 0x01 B[5:4]	Resolution (pixel count)
00	720P (1280 x 720)
01	1080P (1920 x 1080)
10	Full Resolution (2591 x 1944)
11	VGA (640 x 480)

7.1.2.1 Region of Interest (RIO)

In the case of the 720P and VGA display modes, there are two options for displaying the reduced resolution image. The first option is to display only that part of the image corresponding to the reduced pixel count. In this case, only the central part of the image will be displayed as shown in Figure 7.

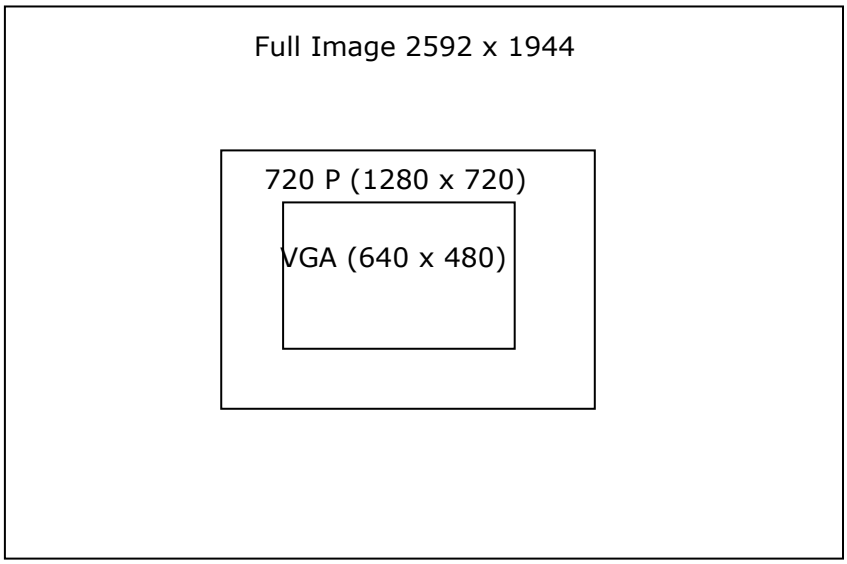


Figure 7. Region of Interest Display (720 P and VGA modes only)

The second option is to display the entire image with reduced resolution, this is done using either pixel binning or line column skipping as described below.

7.1.2.2 Binning Row/Column skipping

Binning and row/column skipping can be used to display the full screen image at a reduced resolution. With Binning, the reduced resolution image is created by summing adjacent pixels in either 2x2 or 4x4 blocks to create the 720P and VGA formats respectively.

In the case of row and column skipping, the reduced resolution image is produced simply by skipping the appropriate number of rows and columns.

Binning has the advantage that the sensitivity of the camera is increased by effectively enlarging the size of the pixel.

The two display modes are illustrated in Figure 8

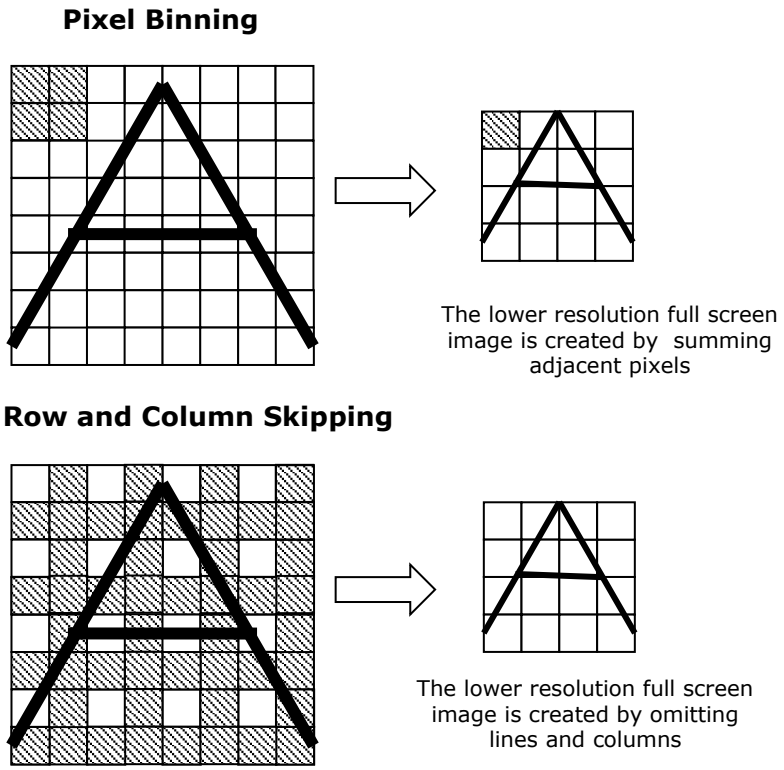


Figure 8. Binnig and Row/Column Skipping

The display mode is controlled via register 0x01 B[1:0] as shown in Table 9

Table 9. Display mode settings (720P and VGA only)

Reg 0x01 bits[1:0]	Display Mode
00 or 11	Region Of Interest (ROI)
01	Binning
10	Row/Column Skipping

7.1.3 Flickerless Operation

The camera can be put in a 50Hz or 60Hz mode. This is to reduce the flicker that can result when using the camera under artificial lighting that is operating on either a 50HZ or 60Hz frequency.

The frequency settings is controlled via bit[7] of register 0x01 and results in slightly different frame rates for the 50 and 60 Hz options as shown in Table 10.

Table 10. Frequency Settings

Reg 0x01 bit[7]	Frequency	Frame rates (Resolution)
0	60 Hz	Full resolution 5Mpixel: 14.6 fps 1080P: 30 fps 720P: 60 fps / 55 fps for binning/skipping VGA: 120 fps
1	50 Hz	Full resolution 5Mpixel: 12.5 fps 1080P: 25 fps 720P: 50 fps VGA: 100 fps

7.1.4 Image orientation

Horizontal and vertical mirror images can be selected via bits[1:0] of register 0x05 as shown in the table below.

Reg 0x05 bits[1:0]	Image Orientation
00	Normal
01	Horizontal Mirror
10	Vertical Mirror (FLIP)
11	Vertical & Horizontal Mirror

7.1.5 Edge enhancement

The camera is also equipped with an edge enhancement feature which can be used to create sharper edges, giving the appearance of higher resolution. See Figure 9
The edge enhancement mode is controlled by register 0x06.
The following bits are used:

- bit[0] activates the edge enhancement: 1 = ON, 0 = OFF.
- bits[3:2] sets the grade of the edge enhancement. Next tastes can be set:
  00 is standard, 01= Boost 2x, 10= Boost 4x, 11 = Boost 8x.

Note: It is not recommended to use the boost 4x or 8x.

Register 0x07 sets the gain of the sharpness ranging from 0(=off) to 0xFF(=maximum).
Note that in addition to providing a sharper looking image, the edge enhancement feature will also accentuate the noise. To compensate for this, the camera has an edge suppression mode, which automatically reduces the Edge Enhancement when the AGC level exceeds a starting point. The rate of reduction occurs in a linear way as the AGC level increases until the end point is reached. At this point the gain of sharpness will be zero.

The starting point can be set with register 0x08. The set value ranges from 0x00 to 0xB1 and matches the setting as used for register 0x03 (manual gain control). Therefore to use a specific AGC level, apply a lookup into the *total gain* column of the *table 7 Fixed Gain settings* and use the appropriate gain setting in column 1.

The end point can be set with register 0x09. The set value ranges from 0x01 to 0xB2. To apply a specific AGC level, use the matching set value as denoted in the table 7 as explained for the starting level.
Note that the end point must be greater than the start point.

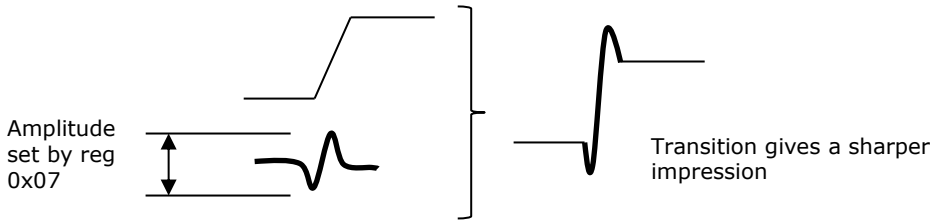
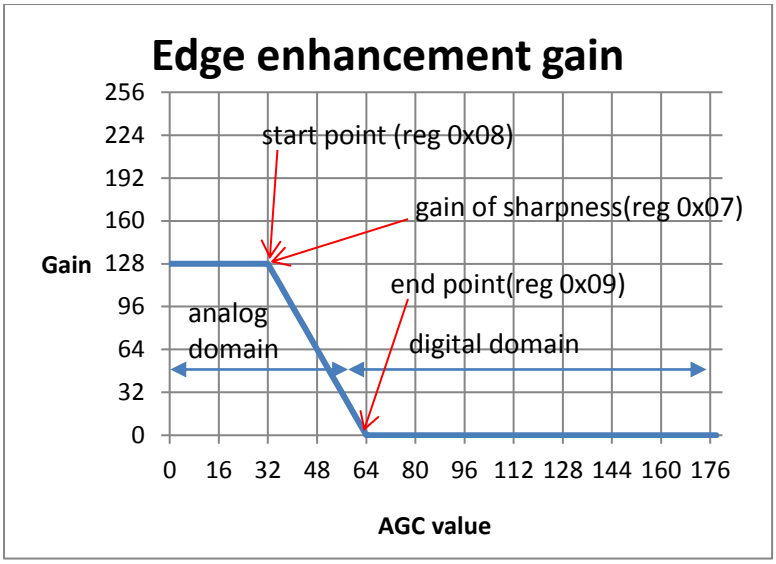


Figure 9. Edge enhancement

The next figure illustrates the gain for the default settings as a function of the AGC value (the AGC value is the transposed value for the actual AGC level as per table 7).



7.1.6 Contrast control

Register 0x0D controls the overall contrast (Y-gain) of the image.
The range is from 0x00 (low) to 0xFF(high).
Value 0x80 is the middle (default) value. A value in the range 0x81 to 0xFF will result in an increase of the contrast and a value in the range 0x00 to 0x7F will result in a decrease of the contrast.

7.1.7 Brightness control

Register 0x15 controls the overall brightness (Y-offset) of the image.
The range is from 0x00 (low) to 0xFF(high).
Value 0x80 is the middle (default) value. A value in the range 0x81 to 0xFF will result in an increase in brightness and a value in the range 0x00 to 0x7F will result in a decrease in brightness.

7.1.8 Back Light Compensation (BLC) mode

Back Light Compensation is used to improve the image quality when the subject is illuminated from behind such as when standing in front of a brightly lit window.

Normally the auto-exposure control would reduce the gain to keep all parts of the image within the desired range; this would result in the subject becoming a silhouette as shown in Figure 10.

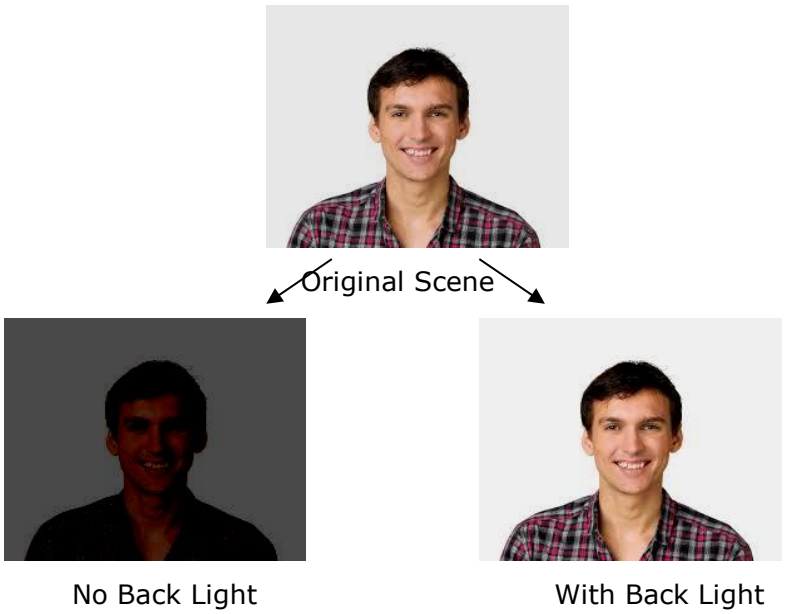


Figure 10. Effect Of Back Light Compensation

The BLC works by assigning more priority to a certain part of the image - the BLC Window.
The part of the image within this window is then given an extra weighting compared with remaining window when determining the exposure and gain values.

The BLC feature is activated by setting bit[0] of register 0x10 B[0] to 1.
(It may also be set via bit bit[2] of register 0x00. In either case the setting will be copied to the other register).

This weighting factor (or BLC-gain) assigned to the BLC window is set via register 0x11.

The weighting factor is employed according to the formula:
The measured average luminance value *avrLum* of the image that is used as reference for controlling the shutter and gain value is employed according next formula:
avrLum = β * *avrWindow* + (1- β) * *avrImage*.

Here *avrImage* and *avrWindow* and are the average luminance values for the window and entire image respectively and the coefficient β is defined as 256/BLC-gain.

So if BLC-gain is set to a minimum of 0, the window has no extra weighting and in case of the maximum BLC-gain of 0xFF, only the window is accounted for the average luminance value. All BLC-gain values in between account for more or less of the remaining part of the image.

For the purpose of defining the BLC window, the camera sensor is divide into an array of 16 x 16 Blocks, as shown in Figure 11.
The size of the window is set via register 0x13. Bits[3:0] define the horizontal size, and bits[7:4] define the vertical size. The size is equal to the value plus 1, so a value of 0 means a size of 1.

The position of the window is set via registers 0x14, with bits[3:0] and bits[7:4] defining the horizontal and vertical location referenced to the top-left corner of the screen.

Two windows are illustrated in Figure 11. The light blue window is the default window.
The window can be viewed by setting bit[7] of register 0x10.
Note: at power-up the viewing option is automatically cleared.

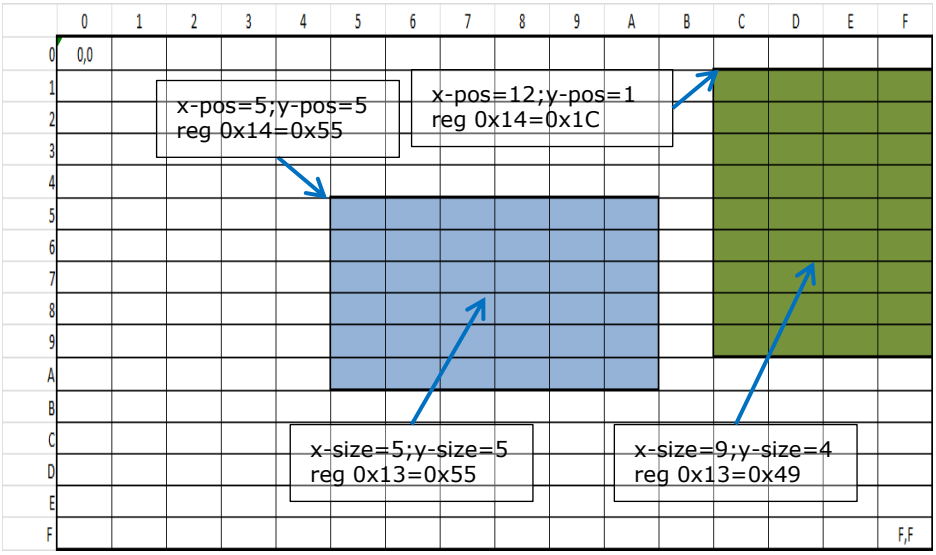


Figure 11. BLC Blocks

7.1.9 Gamma correction

The camera has a built in gamma correction. The gamma correction factor can be set between 0.45 and 1 in steps of 0.05.

Register 0x70 can be set ranging from 0x00 (gamma = 0.45) to 0x0B (gamma = 1.0).

7.1.10 2D Noise Reduction

Under low-light conditions, the gain is set and introduces visible noise in the image. A 2D Noise reduction method is employed to reduce this noise. This method employs a Gaussian filter which combines adjacent pixels (in a 5 x 5 matrix) to compensate for the noise. However a drawback is that it introduces some visual reduction of the resolution (smoothing) and some blurring of object edges. Nevertheless one can make a compromise between both disadvantages.

The 2D noise reduction mode is controlled by bit[0] of register 0x18: 1 = ON, 0 = OFF.

Register 0x19, denoted as 2D-gain, sets the strength of the 2D noise reduction; in fact it sets the standard deviation σ of the Gaussian filter and therefore the width of the Gaussian distribution. The range of the register is from 0(=noise reduction is off) to 0xFF(=equal averaging over 5x5 pixel matrix).

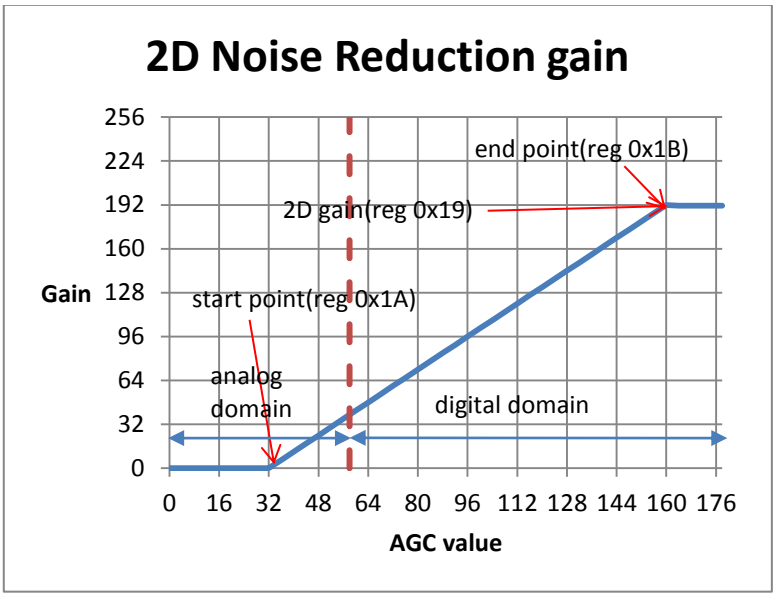
Because applying the filter is dependent on the noise level, which in turn relates to the AGC level, it is obvious that 2D-gain should increase as the AGC level increases.

For this reason an AGC level starting and ending point can be set. The 2D noise reduction will start when the AGC level passes a starting point and increases in strength in a linear way until the AGC level reaches the end point, which corresponds to the final 2D-gain.

The starting point can be set with register 0x1A. The set value ranges from 0x00 to 0xB1 and matches the setting used for register 0x03 (manual gain control). Therefore to use a specific AGC level apply a lookup into the *total gain* column of the *table 7 Fixed Gain settings* and use the appropriate gain setting in column 1.

The end point can be set with register 0x1B. The set value ranges from 0x01 to 0xB2. To apply a specific AGC level, use the matching set value as denoted in the table 7 as explained for the starting level.
Note that the end point must be greater than the start point.

The below figure illustrates the gain for the default settings as a function of the AGC value (the AGC value is the transposed value for the actual AGC level as per table 7).



7.1.11 EEPROM Register Save/Restore command

The user registers can be saved in EEPROM so that that the customer's adjusted settings are loaded upon power-up.

Additionally a command is needed to reset the settings to the factory defaults.
Both features are supported with the register 0x50 using next values:

Value = 1: Save current settings in user setting area (= EEPROM page 0).
This means that after a repower, settings will be the same.

Value = 2: Set default settings in user setting area (=EEPROM(page0):
This means that the factory settings in EEPROM page 2 is copied to EEPROM page 0.

Note: other values are not accepted.

7.1.12 Password protection

To avoid accidental writing to the sensor and FPGA registers, some other privileged registers and EEPROM locations, certain registers are password protected. Access is only granted after setting unique password values into the two Password registers.

Remark: after a repower the password is lost.

Some function registers are not accessible unless the correct password values are written into the register addresses 0xFC and 0xFD. The order in which both values are written is not important as long as both are entered correctly in succession.

The following registers are access protected:

- All sensor and FPGA registers (only write protected)
- All EEPROM registers for page 1, 2 and 3 (0xA2 ~0xA7) (only write protected)
- EEPROM registers ranges for page 0 (0xA0/0xA1) (only write protected):
    - 0x00~0x6F which are not EEPROM recovered user registers
    - 0x70~0xBF (includes calibration registers 0x70 ~0x7F)
    - 0xF0~0xFF

    Remark: registers ranging from 0xC0 to 0xEF is a user free area

7.1.13 Microcontroller Software Version

The Software Version of the Microcontroller can be read via register 0xFF. The value Bits[7:4] of the value is the Major number; bits[3:0] is the minor number. (example: Data=0x13 means V1.3 (1=major, 3=minor).

7.2 Register Summary

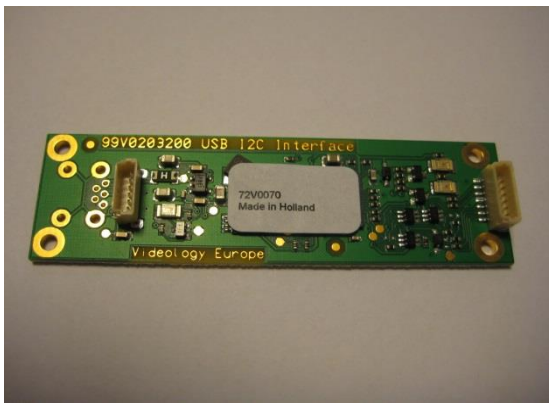
A complete list of the control registers is given in Table 11.

Table 11. Register Listing

Reg.	range	Function description (per bit)	Default value
0x00	0x00-0x7f	AEX mode 1: B[1:0]: AEX/manual mode B[3:2]: 01 =BLC mode on, other = off B[6:4]: fixed shutter speed in steps of ⅛ of frame time B[7] not used	0x04
0x01	0x00-0xff	Resolution mode B[1:0] : mode ROI/Binning/Skipping (for 720P and VGA) B[5:4]: set resolution (720P/1080P/ 5MP/ VGA) B[7] : 0= 60Hz mode, 1 = 50Hz mode	0x20
0x02	0x00-0xff	AEX mode 2 B[6:4]: AEX speed: time constant control loop (400ms steps) B[7]: in case of fixed shutter , fine control via reg 0x12.	0x10
0x03	0x00-0xff	Manual gain value	0x00
0x04	0x00-0xff	AEX Reference level	0x80
0x05	0x00-0x03	Image orientation B[0] = mirror, B[1] = flip	0x00
0x06	0x00-0x01	Edge enhancement mode on/off bit[0]: Mode: 0=OFF; 1=ON; bit[3:2]: Boost: 00=STD, 01=2x; 10=4x; 11=3x	0x01
0x07	0x00-0xff	Edge enhancement gain	0x80
0x08	0x00-0xff	Edge enhancement AGC start suppression	0x18
0x09	0x00-0xff	Edge enhancement AGC end suppression	0x40
0x0b	0x00-0xff	AEX hysteresis reference level	0x10
0x0C	0x00-0xff	Max AGC gain (analog: 0x00-0x3A; dig 0x3A~0xB2)	0x3a
0x0D	0x00-0xff	Contrast	0x80
0x10	0x00-0x01	BLC mode: B[0]: 0 = OFF; 1 = ON (is copied to reg 0x00 B[3:2]) B[7]: show BLC window (only effective for BLC is ON)	0x01
0x11	0x00-0xff	BLC weight factor	0x80
0x12	0x00-0xff	Fixed shutter speed (fine control), steps of 8 lines	0x40
0x13	0x00-0xff	BLC window size B[3:0] size in horizontal direction B[7:4] size in vertical direction	0x55
0x14	0x00-0xff	BLC window position B[3:0] pos in horizontal direction B[7:4] pos in vertical direction	0x55
0x15	0x00-0xff	Brightness control: 0x00 is lowest; 0x80 is mid; 0xFF is highest	0x80
0x16	0x00-0x05	USB output mode (do not use)	0x00
0x17	0x00-0x11	Gamma Correction (0,45, 0,5 …. 1,0)	0x00
0x18	0x00-0x01	2D NR mode on/off	0x01
0x19	0x00-0xff	2D NR gain	0xC0
0x1A	0x00-0xB1	2D NR AGC start point	0x20
0x1B	0x00-0xB2	2D NR AGC end point	0xA0
0xff	RO	Software revision number	RO

8. Communication

To communicate with the camera Videology offers a communication kit (type number tbd) and control software.
The communication kit is an USB2.0 communication board to I2C (see below)



In case of the USB3 version of the camera (25B5.0xUSB3), communication is also possible via the Videology USB 3 viewer. For more details please see the USB3 SDK from Videology

9. Contact Information

For technical assistance with this product, please contact the supplier from whom the product was purchased.

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