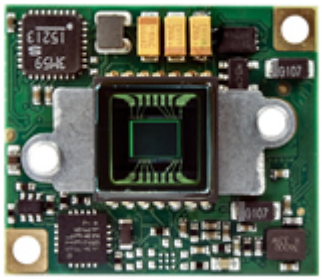
VIDEOLOGY

IMAGING SOLUTIONS INC.

Original Equipment Manufacturer

Application Note
20D05x/ 21D05x
20D15x/ 21D15x
20D17x/ 21D17x
20K17x/ 21K17x



2XK17X (1/4” CCD Color)

2XD17X (1/3” CCD Color)
2XD05X (1/3” CCD B&W)
2XD15X (1/3” CCD Color)

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Videology® Imaging Solutions, Inc.
37M Lark Industrial Parkway
Greenville, Rhode Island 02828 USA
Tel: (401) 949 – 5332 Fax: (401) 949 – 5276
Americas, Middle East, Far East & Australia sales:
sales@videologyinc.com

Videology® Imaging Solutions, Europe B.V.
Neutronenlaan 4
5405 NH Uden, The Netherlands
Tel: +31 (0) 413 256261 Fax: +31 (0) 413 251712
Europe & N. Eurasia sales:
info@videology.nl

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Table of Contents

1 Document History

Revision	Issue Date	Reason	CN#
Rev D	26-mar-2018	Spectral response for 20D05X section 11, section 4 specs updated	18-0026
Rev C	17-mar-2017	Specs updated on all models. Section 4	17-0025
Rev B	07-jun-2016	Initial Release, Formatted for public, Removed model 2xD07, 2xD15, Section 4 – specs updated Section 5 - Connectors, updated to correct pin 1 placement, Section 10 - I2C instructions updated	16-0059
Rev 1.6	06-may-2016	Verified/updated specs 21D15 model	-
Rev 1.5	05-feb-2016	Add I^2C communication kit 60K1A	-
Rev 1.4	28-jan-2016	Add 2XD17, 2XD07 and 2XD05 models, Add blemish sensitivity and high luminance color suppression settings	-
Rev 1.3	11-jan-2016	Add B/W camera notes. P2W description modification	-
Rev 1.2	03-dec-2015	Add push-to-white function	-
Rev 1.1	02-dec-2015	I^2C protocol description modification	-
Rev 1.0	23-nov-2015	Pin change hardware	-
Rev 0.9	12-okt-2015	Add color edge suppression gain	-
Rev 0.8	28-sep-2015	Add black/white - color settings	-
Rev 0.7	15-jul-2015	Review modifications	-
Rev 0.6	15-jul-2015	Draft for initial review	-

2 Product Features

- 1/4" Color CCD sensor with 610k pixels for PAL & 520k pixels for NTSC (2xK17x models)
- 1/3" Color CCD sensor with 610k pixels for PAL & 520k pixels for NTSC (2xD17x models)
- 1/3" Color CCD sensor with 470k pixels for PAL & 410k pixels for NTSC (2xD15x models)
- 1/3" B/W CCD sensor with 470k pixels for CCIR & 410k pixels for EIA (2xD05x models)
- Low noise and low blooming
- Provides analog (CVBS) and digital (BT.656) video output simultaneously
- Automatic blemish detection and compensation process
- Miniature rugged 22mm x 26mm single board (2xK17x models)
- 32mm x 32mm single board (2xD17x/ 2xD05x models)
- Software controllable features and functions
- Lens Mounts: Metal CS, M12 Board or Pinhole

3 Introduction

The 2XK17X, 2XD17X, 2XD15X and 2XD05X is a CCD based camera family with an analog and digital output (BT.656 based).

For the 2XK17X family the dimensions are 26*22mm with 2 mounting holes (dimensions and electrical connections are compatible with the predecessor cameras being 2xK13X(DIG), 2xK14X(DIG) and 2xK15X(DIG) camera family).

For the 2XD17X, 2XD15X and 2XD05X families the dimensions are 32*32mm with 4 mounting holes (dimensions and electrical connections are compatible with the predecessor cameras 2xD20X camera family).

Communication is possible via I^2C. The digital output has been described fully in this document. The camera can also be connected can the 30-pin board-to-board connector. This 30-pin board-to-board connector can be used to "piggy-back" to an application interface circuit board.

This document is written to give technical background on this camera module and all the connectors are being described in this application note.

4 Specifications

4.1 20D05X / 21D05X

Electrical

Image sensor	1/3” CCD B/W	
Active Pixels (H x V)	EIA: 768 x 494	CCIR: 752 x 582
Shutter Mode	Global (Interlaced)	
Resolution	720H	
Sensitivity	< 0.005 Lux F.2 @ 20 IRE < 0.0005 Lux F.2 @ 50 IRE	
Signal to Noise ratio	51 dB ±0.5	
Video Output	Digital 8-bits BT.656 Composite 1Vp-p CVBS (75 ohms)	
Supplied Voltage	5VDC – 15VDC+/- 5%	
Power Consumption	≤1.0W	

Controls

Serial interface	Two wire data/clock up to 100kHz
Shutter speeds	EIA: Automatic from 1/60 to 1/100,000 CCIR: Automatic from 1/50 to 1/100,000 11 fixed speeds via software
Mirror mode	Default off; selectable via software
Back Light Compensation	Default off: selectable via software
Gamma	0.45, fixed
AGC control	Automatic 36 dB (AGC default) or fixed options via software
White Balance Mode	AWB auto (default); other modes selectable via software

Environmental

Operating Temp.	-10º ~ 50º Celsius (14°F ~ 122°F)
Operating Humidity	30% ~ 90% RH
Storage Temp.	-40º ~ 70º Celsius (-40°F ~ 158°F)
Storage Humidity	85% RH
Life time MTBF	> 150,000 hrs.

Mechanical

Dimensions WxHxD	32 x 32 x 14 mm (1.26” x 1.26” x 0.55”) without lens mount 32 x 32 x 24 mm (1.26” x 1.26” x 0.95”) with M12 lens mount
Weight	6.2 gram without lens mount 15.8 gram with M12 lens mount
Lens mount	Replace “X” in model number with desired lens mount: • 2: Metal pinhole lens mount • 5: Metal M12 board lens mount • 7: no lens mount • 8: Metal CS lens mount
Connectors	J100: 6 pin connector JST BM06B-SRSS (I^2C, CVBS, PSU) J101: 30 pole B2B connector Molex 501920-3001 (digital output)

Accessories

Optional I^2C (60K5-U)	Software control I^2C program kit includes: I^2C board, Program cable, USB cable, Camera control software (SFT-15521)

4.2 20D15X / 21D15X

Electrical

Image sensor	1/3” CCD Color	
Active Pixels (H x V)	NTSC: 768 x 494	PAL: 752 x 582
Shutter Mode	Global (Interlaced)	
Resolution	720H	
Sensitivity	0.1 Lux (30 IRE), < 0.25 Lux (50 IRE)	
Signal to Noise ratio	50 dB	
Video Output	Digital 8-bits BT.656 Composite 1Vp-p CVBS (75 ohms) YC output (Optional, requires layout change)	
Supplied Voltage	5VDC – 15VDC+/- 5%	
Power Consumption	≤1.0W	

Controls

Serial interface	Two wire data/clock up to 100kHz
Shutter speeds	NTSC: Automatic from 1/60 to 1/100,000 PAL: Automatic from 1/50 to 1/100,000 11 fixed speeds via software
Mirror mode	Default off; selectable via software
Back Light Compensation	Default off: selectable via software
Gamma	0.45, fixed
AGC control	Automatic 36 dB (AGC default) or fixed options via software
White Balance Mode	AWB auto (default); other modes selectable via software

Environmental

Operating Temp.	-10º ~ 50º Celsius (14°F ~ 122°F)
Operating Humidity	30% ~ 90% RH
Storage Temp.	-40º ~ 70º Celsius (-40°F ~ 158°F)
Storage Humidity	85% RH
Life time MTBF	> 150,000 hrs.

Mechanical

Dimensions WxHxD	32 x 32 x 14 mm (1.26” x 1.26” x 0.55”) without lens mount 32 x 32 x 24 mm (1.26” x 1.26” x 0.95”) with M12 lens mount
Weight	6.2 gram without lens mount 15.8 gram with M12 lens mount
Lens mount	Replace “X” in model number with desired lens mount: • 2: Metal pinhole lens mount • 5: Metal M12 board lens mount • 7: no lens mount • 8: Metal CS lens mount
Connectors	J100: 6 pin connector JST BM06B-SRSS (I^2C, CVBS, PSU) J101: 30 pole B2B connector Molex 501920-3001 (digital output)

Accessories

Optional I^2C (60K5-U)	Software control I^2C program kit includes: I^2C board, Program cable, USB cable, Camera control software (SFT-15521)

4.3 20D17X / 21D17X

Electrical

Image sensor	1/3" CCD	
Active Pixels (H x V)	NTSC: 976 x 494	PAL: 976 x 582
Shutter Mode	Global (Interlaced)	
Resolution	960H	
Sensitivity	0.1 Lux (30IRE), < 0.25 Lux (50 IRE)	
Signal to Noise ratio	50 dB	
Video Output	Digital 8-bits BT.656 Composite 1Vp-p CVBS (75 ohms)	
Supplied Voltage	5VDC – 15VDC +/- 5%	
Power Consumption	≤1.0W	

Controls

Serial interface	Two wire data/clock up to 100kHz
Shutter speeds	NTSC: Automatic from 1/60 to 1/100,000 PAL: Automatic from 1/50 to 1/100,000 11 fixed speeds via software
Mirror mode	Default off; selectable via software
Back Light Compensation	Default off: selectable via software
Gamma	0.45, fixed
AGC control	Automatic 36 dB (AGC default) or fixed options via software
White Balance Mode	AWB auto (default); other modes selectable via software

Environmental

Operating Temp.	-10º ~ 50º Celsius (14°F ~ 122°F)
Operating Humidity	30% ~ 90% RH
Storage Temp.	-40º ~ 70º Celsius (-40°F ~ 158°F)
Storage Humidity	85% RH
Life time MTBF	> 150,000 hrs.

Mechanical

Dimensions WxHxD	32 x 32 x 14 mm (1.26" x 1.26" x 0.55") without lens mount 32 x 32 x 24 mm (1.26" x 1.26" x 0.95") with M12 lens mount
Weight	6.2 gram without lens mount 15.8 gram with M12 lens mount
Lens mount	Replace "X" in model number with desired lens mount: • 2: Metal pinhole lens mount • 5: Metal M12 board lens mount • 7: no lens mount • 8: Metal CS lens mount
Connectors	J100: 6 pin connector JST BM06B-SRSS (I^2C, CVBS, PSU) J101: 30 pole B2B connector Molex 501920-3001 (digital output)

Accessories

Optional I^2C (60K5-U)	Software control I^2C program kit includes: I^2C board, Program cable, USB cable, Camera control software (SFT-15521)

4.4 20K17X / 21K17X Standard basic features:

Electrical

Image sensor	1/4" CCD	
Active Pixels (H x V)	NTSC: 976 x 494	PAL:976 x 582
Shutter Mode	Global (Interlaced)	
Resolution	960H	
Sensitivity	0.1 Lux (30 IRE), < 0.3 Lux (50 IRE)	
Signal to Noise ratio	50 dB	
Video Output	Digital 8-bits BT.656 Composite 1Vp-p CVBS (75 ohms)	
Supplied Voltage	5VDC – 15VDC	
Power Consumption	≤0.9W	

Controls

Serial interface	Two wire data/clock up to 100kHz
Shutter speeds	NTSC: Automatic from 1/60 to 1/100,000 PAL: Automatic from 1/50 to 1/100,000 11 fixed speeds via software
Mirror mode	Default off; selectable via software
Back Light Compensation	Default off: selectable via software
Gamma	0.45 default
AGC control	Automatic 36 dB (AGC default) or fixed options via software
White Balance Mode	AWB auto (default); other modes selectable via software

Environmental

Operating Temp.	-10° ~ 50° Celsius (14°F ~ 122°F)
Operating Humidity	30% ~ 90% RH
Storage Temp.	-40° ~ 70° Celsius (-40°F ~ 158°F)
Storage Humidity	85% RH
Life time MTBF	> 150,000 hrs

Mechanical

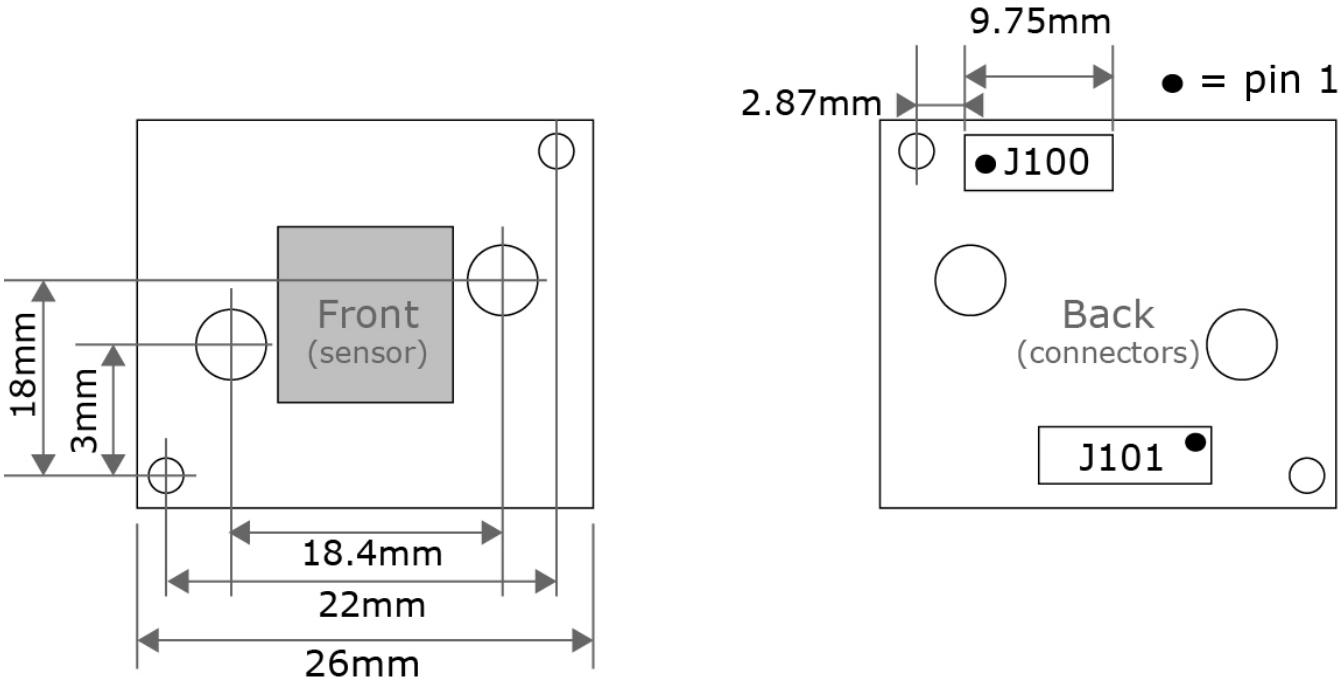
Dimensions WxHxD	26 x 22 x 14 mm (1" x 0.87" x 0.55") without lens mount 26 x 22 x 24 mm (1" x 0.87" x 0.95") with M12 lens mount
Weight	5.4 gram without lens mount 15 gram with M12 lens mount
Lens mount	Replace "X" in model number with desired lens mount: • 2: Metal pinhole lens mount • 5: Metal M12 board lens mount • 7: no lens mount • 8: Metal CS lens mount
Connectors	J100: 6 pin connector JST BM06B-SRSS (I^2C, CVBS, PSU) J101: 30 pole B2B connector Molex 501920-3001 (digital output)

Accessories

Optional I^2C (60K5-U)	Software control I^2C program kit includes: I^2C board, Program cable, USB cable, Camera control software (SFT-15521)

5 Connectors / Interface

5.1 20K17x / 21K17x



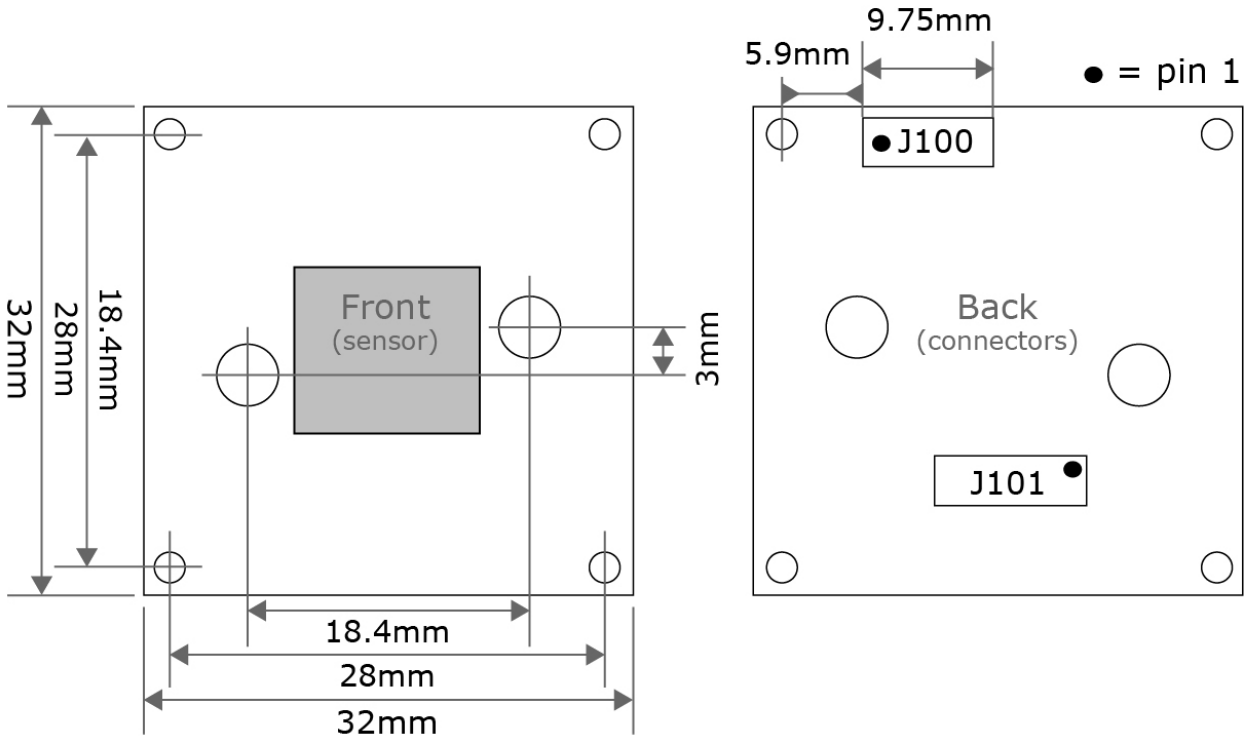
Connector J100 is the main connector for operating the analog camera. Here it can be powered and the single sided CVBS video-out is available. Via the optional cable 60C1045 the camera can be controlled through I^2C See Section 10 USB-I^2C interface tool.

Connector J100 (Top Mount)	
Pin #	Pin name
1	5VDC-15VDC in
2	GND
3	CVBS
4	GND
5	I^2C-SCL
6	I^2C-SDA

Connector J101 is the connector to be used for digital output according ITU-R BT.656. See the table below for the pin description.

Pin #	Pin name	Pin #	Pin name
1	GND	16	
2	GND	17	DOUT7
3	DOUT0	18	
4		19	CLOCKOUT
5	DOUT1	20	
6		21	
7	DOUT2	22	GND
8		23	HSYNC
9	DOUT3	24	VSYNC
10		25	
11	DOUT4	26	
12		27	I^2C-SDA
13	DOUT5	28	I^2C-SCL
14		29	CVBS OUT (analog)
15	DOUT6	30	POWER IN 5-15VDC

5.2 20D05x/ 21D05x, 20D15x/ 21D15x, 20D17x/ 21D17x



Connector J100 is the main connector for operating the analog camera. Here it can be powered and the single sided CVBS video-out is available. Via the optional cable 60C1045 the camera can be controlled through I^2C See Section 10 USB-I^2C interface tool.

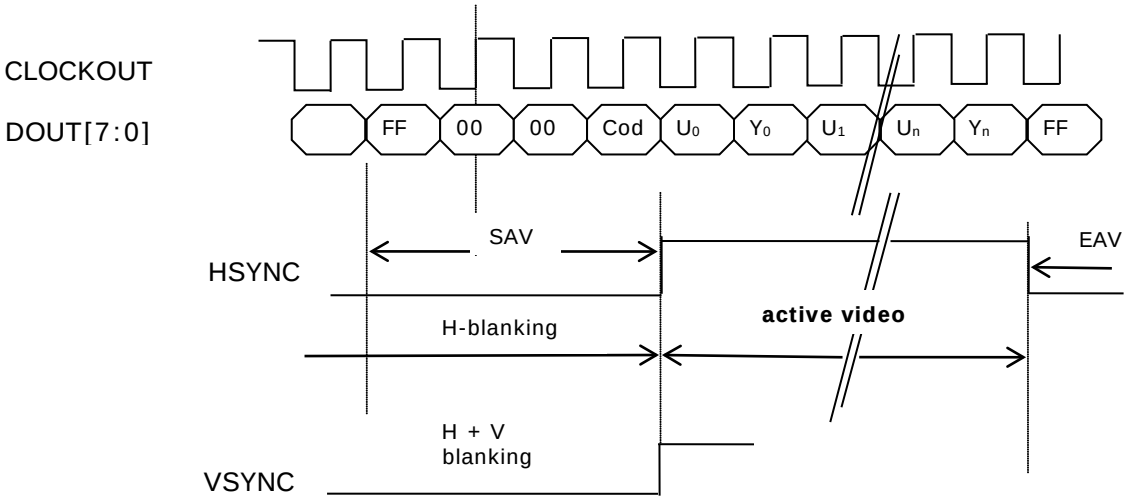
Connector J100 (Top Mount)	
Pin #	Pin name
1	5VDC-15VDC in
2	GND
3	CVBS
4	GND
5	I^2C-SCL
6	I^2C-SDA

Connector J101 is the connector to be used for digital output according ITU-R BT.656. See the table below for the pin description.

Pin #	Pin name	Pin #	Pin name
1	GND	16	
2	GND	17	DOUT7
3	DOUT0	18	
4		19	CLOCKOUT
5	DOUT1	20	
6		21	
7	DOUT2	22	GND
8		23	HSYNC
9	DOUT3	24	VSYNC
10		25	
11	DOUT4	26	
12		27	I^2C-SDA
13	DOUT5	28	I^2C-SCL
14		29	CVBS OUT (analog)
15	DOUT6	30	POWER IN 5-15VDC

6 BT.656 Timing

The BT.656 standard has one bus of 8 bits (DOUT7 ~ DOUT0).
The timing relationship between pixel clock (CLOCKOUT), blanking outputs (HSYNC and VSYNC) and synchronization data is shown in next figure:



The synchronization code is a combination of 4 bytes. The first three bytes are always the same. The sequence is [0xFF], [0x00] and [0x00]. The values 0xFF and 0x00 will not occur in the normal video. The fourth byte (Cod) gives the synchronization position. It uses 3 different signals: FIELD, VD and HD. The last 4 bits contain a protection code to check if an error occurred during the transfer of this position code's byte.

Function	Bit 7:	Bit 6: FIELD	Bit 5: V	Bit 4: H	Bit 3: P3	Bit 2: P2	Bit 1: P1	Bit 0: P0
0	1	0	0	0	0	0	0	0
1	1	0	0	1	1	1	0	1
2	1	0	1	0	1	0	1	1
3	1	0	1	1	0	1	1	0
4	1	1	0	0	0	1	1	1
5	1	1	0	1	1	0	1	0
6	1	1	1	0	1	1	0	0
7	1	1	1	1	0	0	0	1

V = 1 during field blanking; V = 0 elsewhere. H = 1 in EAV; H = 0 in SAV.

	Nominal frequency	Tolerance +/-
CLOCKOUT	36 MHz (All 960H) 28,636 Mhz (720H CCIR/PAL) 28,375 Mhz (720H EIA/NTSC)	20 ppm

7 I²C camera Control

7.1 I²C Protocol for the camera

The camera has a serial communication interface (I²C) provided by the I²C-SCL and I²C-SDA lines. This serial bus has a line for the clock signal and a line for the data signal. The camera will act as a slave device on the bus.

The protocol support clock speeds from 1kHz – 100kHz.

The default camera address is 0x70/0x71. An alternative camera address can be set with command register 0x31. EEPROM page 1 (address = 0xa2) at register address = 0x90; the new address is only applied after repowering.

The communication protocol exists of two blocks. The first block is the command block, followed by the data block.

The command block is always 4 bytes long. It contains the camera address (write only = 0x70), a mode byte, device address and register address.

The Data block is either read or write. This is indicated by the camera address, write is 0x70 and read is 0x71. The least significant bit of the mode byte in the command block also indicates a read or write action (this bit should be 0 for a write and a 1 for a read).

Note that there is a minimal delay time required between the command and data block or data block and successive command block. This delay depends on the direction of communication (write or read).
For a write action to the EEPROM a delay time of at least 10msec. is needed between successive command/data block pairs.

A wait time is also required between commands, so that the internal communication has time to execute the required internal communication. The delay time between the commands should be at least 20msec.

Between Command Block and Data block apply a Delay1 with a minimal value of:

- 150 µs in case the mode byte (in command block) indicates a write
- 1.5 ms in case of a read action (again indicates by the mode byte inside the command block).

Between Data block and next Command Block apply a Delay2 with a minimal value of:

- 10ms for a write action to the EEPROM.
- 50ms for a write action to the command register (this is required for handling the command internally).
- 1.0 ms for all read actions.

7.2 The Command Block

This block is 4 bytes.

Note: Gray blocks is slave controlled data.

Command block									
start	Cam addr W	A	Mode byte r/w	A	Dev addr	A	Reg addr	A	stop

A= acknowledge

- 1st byte is camera address, only valid value is the camera write address, default 0x70
- 2nd byte is the mode byte. The mode byte tells the camera is the host wants to read or write to the camera. If the host wants to read the LS-bit is 1. Valid values can be found in the following table.

Mode byte in command block : valid values	
0x00	Default mode write: commands and access to EEPROM
0x01	Default mode read: commands and access to EEPROM
0x80	DSP access: write
0x81	DSP access: read

- 3rd byte is the device address inside the camera.
  Valid values can be found in the table below:

Device address		
Mode value (2nd byte)	Address value	description
0x00/0x01	0x30/0x31	Command access
	0xa0/0xa1	EEPROM 1st page
	0xa2/0xa3	EEPROM 2nd page
	0xa4/0xa5	EEPROM 3rd page
	0xa6/0xa7	EEPROM 4th page
0x80/0x81	0x00	Access DSP registers 0x000~0x0FF
	0x01	Access DSP registers 0x100~0x1FF
	0x02	Access DSP registers 0x200~0x2FF
	0x03	Access DSP registers 0x300~0x3FF
	0x04	Access DSP registers 0x400~0x4FF
	0x05	Access DSP registers 0x500~0x5FF
	0x06	Access DSP registers 0x600~0x6FF
	0x07	Access DSP registers 0x700~0x7FF
	0x08	Access DSP-EEPROM page 0
	0x09	Access DSP-EEPROM page 1
	0x0A	Access DSP-EEPROM page 2
	0x0B	Access DSP-EEPROM page 3
	0x0C	Access DSP-EEPROM page 4
	0x0D	Access DSP-EEPROM page 5
	0x0E	Access DSP-EEPROM page 6
	0x0F	Access DSP-EEPROM page 7

- 4th byte is the register address. This byte can have any value between 0x00 and 0xff.

7.3 The Data block

This block is always 2 bytes.
The difference here is that the camera can either send or receive data via this block.
Note: Gray blocks are slave controlled data

In case the host sends data to the camera:

Data block: data from host to camera					
start	Cam addr W	A	data	A	stop

A= acknowledge

In case the camera has to send data to the host:

Data block: data from host to camera					
start	Cam addr R	A	data	NA	stop

NA = Not acknowledge

Note: Cam addr W = 0x70; Cam addr R = 0x71.

7.4 Access control

Not all registers are standard accessible in user mode.

A protection mechanism is implemented to avoid that preserved registers are accidentally changed, which could cause unpredictable behavior of the camera or possibly damage the camera.

For special cases the overall protection can be disabled when the correct password values are written into the camera registers 0xFC and 0xFD (remark: the password will only be released in special cases). Hereafte write access to the protected area is permitted.

The next list presents all registers and the accessibility.

	Read Access	Write access	Protected area
EEPROM page 0 (user settings)	0x00 ~ 0xFF	0x00 ~ 0xF7	0xF8 ~ 0xFF
EEPROM page 1 (user free area)	0x00 ~ 0xFF	0x00 ~ 0xFF	None
EEPROM page 2 (factory settings)	0x00 ~ 0xFF	none	0x00 ~ 0xFF
EEPROM page 3 (reserved)	0x00 ~ 0xFF	none	0x00 ~ 0xFF
DSP registers; all 8 banks	none	none	0x000 ~ 0x7FF
DSP EEPROM; all 8 pages	none	none	0x000 ~ 0x7FF

7.5 I^2C registers

The camera has several command registers that allow the user to customize the behavior of the camera. For every command register there is an identical EEPROM location too. When a command register value should be applied after repowering it is necessary to write the same value to the EEPROM device at the location matching the command register. The result of this is, that this new setting will be recovered after the next power-up. In this way the EEPROM device contains all customized standard settings.
In case the default (factory) settings should be used again, a special command register (0xf0) is provided.

(Note: there is a possibility to access the DSP registers via the I^2C interface, but this is restricted information due to its complex structure and is password protected).

In this document only the command registers will be addressed as well as the EEPROM mapping.
The I2C registers are listed below.
In the Detailed Register Information paragraph a more detailed description can be found.

7.6 Register Overview

Device address (w/r)	Register address	function
0x30/0x31	0x01	Camera Identification (read only)
0x30/0x31	0x02	AGC control Auto/Fixed
0x30/0x31	0x04	Control register: Mirror, shutter speed selection, White Balance Mode (=WB mode)
0x30/0x31	0x05	Minimum and Maximum shutter speed limits
0x30/0x31	0x06	Exposure control target (AEX ref point) for normal use (BLC off)
0x30/0x31	0x09	Exposure control target (AEX ref point) for normal use (BLC On)
0x30/0x31	0x13	BLC mode
0x30/0x31	0x1B	AGC upper limitation
0x30/0x31	0x1C	AGC lower limitation
0x30/0x31	0x1D	Fixed Gain [bit7:0 (LSB)]
0x30/0x31	0x1E	Fixed Gain [bit8 (MSB)]
0x30/0x31	0x31	I2C Camera Address
0x30/0x31	0x33	AWB window weight factor
0x30/0x31	0x34	AWB Position and Size
0x30/0x31	0x42	WB Mode1 (3200K; indoor) Red Gain
0x30/0x31	0x43	WB Mode1 (3200K; indoor) Blue Gain
0x30/0x31	0x44	WB Mode2 (4500K) Red Gain
0x30/0x31	0x45	WB Mode2 (4500K) Blue Gain
0x30/0x31	0x46	WB Mode3 (6300K; outdoor) Red Gain
0x30/0x31	0x47	WB Mode3 (6300K; outdoor) Blue Gain
0x30/0x31	0x48	Chrominance gain of R-Y negative direction for WB1
0x30/0x31	0x49	Chrominance gain of B-Y negative direction for WB1
0x30/0x31	0x4A	Chrominance gain of R-Y positive direction for WB1
0x30/0x31	0x4B	Chrominance gain of R-Y positive direction for WB1
0x30/0x31	0x4C	Chrominance gain of R-Y negative direction for WB2
0x30/0x31	0x4D	Chrominance gain of B-Y negative direction for WB2
0x30/0x31	0x4E	Chrominance gain of R-Y positive direction for WB2
0x30/0x31	0x4F	Chrominance gain of R-Y positive direction for WB2
0x30/0x31	0x50	Chrominance gain of R-Y negative direction for WB3
0x30/0x31	0x51	Chrominance gain of B-Y negative direction for WB3
0x30/0x31	0x52	Chrominance gain of R-Y positive direction for WB3
0x30/0x31	0x53	Chrominance gain of R-Y positive direction for WB3
0x30/0x31	0x54	Chrominance phase B-Y toward R-Y axis in -region for WB1
0x30/0x31	0x55	Chrominance phase R-Y toward B-Y axis in -region for WB1
0x30/0x31	0x56	Chrominance phase B-Y toward R-Y axis in +region for WB1
0x30/0x31	0x57	Chrominance phase R-Y toward B-Y axis in +region for WB1
0x30/0x31	0x58	Chrominance phase B-Y toward R-Y axis in -region for WB2
0x30/0x31	0x59	Chrominance phase R-Y toward B-Y axis in -region for WB2
0x30/0x31	0x5A	Chrominance phase B-Y toward R-Y axis in +region for WB2
0x30/0x31	0x5B	Chrominance phase R-Y toward B-Y axis in +region for WB2
0x30/0x31	0x5C	Chrominance phase B-Y toward R-Y axis in -region for WB3
0x30/0x31	0x5D	Chrominance phase R-Y toward B-Y axis in -region for WB3
0x30/0x31	0x5E	Chrominance phase B-Y toward R-Y axis in +region for WB3
0x30/0x31	0x5F	Chrominance phase R-Y toward B-Y axis in +region for WB3
0x30/0x31	0x60	Day/night mode
0x30/0x31	0x62	Day -> night AGC threshold value
0x30/0x31	0x63	Night -> day AGC threshold value
0x30/0x31	0x64	Day <--> Night delay values
0x30/0x31	0x7B	Vertical and horizontal aperture on/off (Edge enhancement)
0x30/0x31	0x7C	Horizontal aperture gain

0x30/0x31	0x7E	Vertical aperture gain
0x30/0x31	0x80	Blemish Correction sensitivity
0x30/0x31	0x81	Blemish Correction start/clear (write only)
0x30/0x31	0x82	Digital Output control
0x30/0x31	0x83	Digital Y-gain
0x30/0x31	0x84	Digital C-gain
0x30/0x31	0x88	CVBS: Setup Level
0x30/0x31	0x89	CVBS: Burst Level R-Y
0x30/0x31	0x8A	CVBS: Burst Level B-Y
0x30/0x31	0x8B	CVBS: Output Gain
0x30/0x31	0x8C	CVBS: Sync Level
0x30/0x31	0x9C	BLC coefficients Group A and B
0x30/0x31	0x9D	BLC coefficients Group C and D
0x30/0x31	0x9E	BLC coefficients Group E and F
0x30/0x31	0x9F	BLC coefficients Group G and H
0x30/0x31	0xA0	BLC coefficients Group I and J
0x30/0x31	0xA1	BLC coefficients Group K and L
0x30/0x31	0xA6	High luminance color suppression start level
0x30/0x31	0xA7	Color edge suppression gain
0x30/0x31	0xF0	Write default register values in EEPROM and apply these settings
0x30/0x31	0xFC	Password (write only) MSB
0x30/0x31	0xFD	Password (write only) LSB
0x30/0x31	0xFF	Microcontroller Software revision number (read only)

7.7 Password protected registers

Some registers are not accessible unless correct password values are written into the address 0xfc and 0xfd of the command register set.
Next registers are protected:

- All DSP registers, both for read and write access
- EEPROM registers for page 0 in the range of 0xF8~0xFF and all EEPROM registers for page 2 and 3.

Device addr.	Register addr.	Description
0x30 (w)	0xf0	Write default command register values in EEPROM
	0xf1	Read all EEPROM settings and write to command registers
	0xf6	Clear all EEPROM pages (page 0, 1, 2 and 3)

8 Detailed register information

Next each command register is described in detail.

8.1 Camera Identification

This register identifies the type of camera configuration. Next bit definitions are used:
Example: For 21K17x, the value is 0x60.

Device address	Register address	bits	Read only
0x30/0x31 (r)	0x01	[7:0]	0x60(PAL); 0x20(NTSC
Bit[7]: 0=CVBS; 1=YC Bit[6]: 0=NTSC; 1=PAL Bit[5:4]: 00=270/320K; 01=410/470K; 10=520/610K (960H), 11=Reserved Bit[3]: 0=Color; 1= B/W Bit[2]: 0=1/4" Sensor, 1=1/3" Sensor Bit[0]: Reserved			

8.2 I2C Camera Address

Standard the I2C camera address is 0x70. To avoid collision in cases that this address value is already assigned to another slave device on the same bus, an alternative address can be chosen.
When a new value is written to the corresponding EEPROM location in page0 and next the camera is repowered, the camera reacts only on this new address.

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x31	[7:0]	0x70
Camera address (=I^2C address); valid range 0x00 ~ 0xFC			

8.3 AGC control auto/fixed

The camera is equipped with auto exposure control. In some circumstances it is desired that not all the auto loops are running. Therefore the camera has the capability to switch off the auto gain control and set the gain according a fixed value with register 0x1D and 0x1E.

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x02	[1]	0x29
If b[1] = 0: the camera functions with automatic gain control (default) If b[1] = 1: the gain is fixed. Required gain value can be set via register address 0x1D and 0x1E. All other bits are don't care.			

8.4 AGC Fixed

The fixed gain value ranges from 0x000 to 0x17F (383) and thus exists of 9 bits. The least significant 8 bits are set with register 0x1D and the most significant bit is set with bit 3 of register 0x1E.
The gain value can be expressed in dB. A value of 0 = -3.15dB; 0x20(32) = 0dB;
0x40 (64) = 3,40dB … 0x17F (383) = 36 dB
In general the next formula can be used: Gain[dB] = 0,1022 * gain_value – 3,15.

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x1D	[7:0]	0x05
Fixed gain value: bit 7:0 (LSB)			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x1E	[3]	0x00
Fixed gain value: bit 8 (MSB)			

8.5 Control register

With this register the user can control next settings: White Balance, Shutter Speeds and Mirror mode.

8.5.1 White Balance

- Auto white modes (AUTO1 or AUTO2).
- Indoor setting (=3200K), further indicated as WB1
- Fluorescent mode (=4500K), further indicated as WB2
- Outdoor mode (=6400K), further indicated as WB3
- Push-to-white mode (arbitrary fixed color temperature)

Push-to-white and WB1 share the same register set. Figure 1 explains how the memory of this function is implemented.

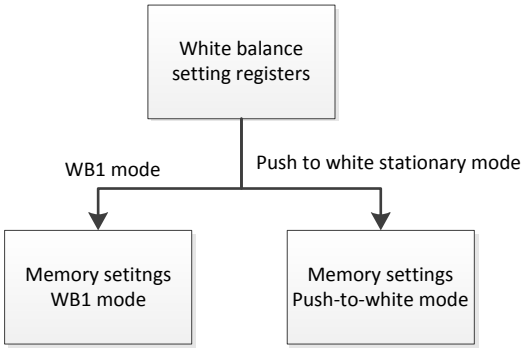


Figure 1

The push-to-white mode exists in two states.
The “set state” will adjust the white balance of the current scene, the “stationary state” uses the new white balance values so the white balance will be fixed.
The camera will automatically go to the “stationary state” once the “set state” has finished adjusting the white balance, this will take about 5 seconds.

In “stationary state” the user is able to adjust the parameters of the white balance via R-gain (register address 0x42), B-gain (register address 0x43), color difference gains (register addresses 0x48 – 0x4B) and color difference phase adjustments (register addresses 0x54 – 0x57) to enhance the picture quality for their application. The “Set push-to-white” mode sets these registers to the appropriate values.

Note: When a “set push-to-white” command is send the camera is not able to communicate for the next 5 seconds.

8.5.2 Shutter Speed

In default mode the camera operates in the electronic iris mode. This means that the CCD output, which is dependent on the light intensity, is controlled by the electronics of the camera and not the mechanics of the lens.

By measuring the output of the CCD and comparing it with an internal reference it is possible to control the output level of the signal out of the CCD (within a certain tolerance).

However, users may in some cases prefer a fixed shutter over an automatic shutter. For example, a fixed shutter is beneficial if there is a very fast moving object in the scene. The longer the integration time (the period that no OFD pulse occurs, max 1/50 sec for PAL and max 1/60 sec for NTSC) the less clear the image will appear due to movement of the object during the integration period. To prevent this from occurring, the camera has 13 fixed shutter speeds.

Besides the manual mode there is a special auto shutter mode available in the camera. In this mode the camera controls the shutter automatically, but the longest and shortest integration time can be set (register 0x05).

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x04	[7], [6:3], [2:0]	0x70

Bit[7]: **mirror mode** (horizontal): bit[7] = 1 mirror; bit[7] = 0 normal output

Bit[6:3] **Shutter Speed**

- 0000 = 1/50(PAL);1/60(NTSC)
- 0001 = 1/120(PAL);1/100(NTSC) (flickerless)
- 0010 = 1/250
- 0011 = 1/500
- 0100 = 1/1000
- 0101 = 1/2000
- 0110 = 1/5000
- 0111 = 1/10000
- 1000 = 1/20000
- 1001 = 1/50000
- 1010 = 1/100000
- 1110 = Auto Limited: Minimum to Maximum shutter speed (register 0x05)
- 1111 = Auto: Minimum shutter speed (register 0x05 bit[7]) to 1/100000

Bit[2:0] **White Balance** mode

- 000 = Auto White Mode (AUTO1)
- 100 = Auto White Mode (AUTO2)
- 001 = Indoor (3200K) WB1
- 010 = Fluorescent(4500K) WB2
- 011 = Outdoor (6400K) WB3
- 101 = Push-to-white (restores values of the last “Set push-to-white” command)
- 110 = Set push-to-white (goes to setting “Push-to-white” after completion)

Note 1: When a “set push-to-white” command is send the camera is not able to communicate for the coming 5 seconds.

Note 2: White balance cannot be set with black/white cameras (2xD05x)

8.6 Minimum and maximum shutter speed limits:

The shutter speed can be understood as an exposure time in milliseconds. When the shutter speed in the control register is set to Auto Limited, the control system will set an exposure time which can vary between 0,01 and 20(PAL) or 16,67(NTSC) milliseconds.

The range of the exposure time area can be limited.

The upper time boundary can be adjusted with the minimum shutter speed limit
Bit 7 of value selects the minimum shutter speed:

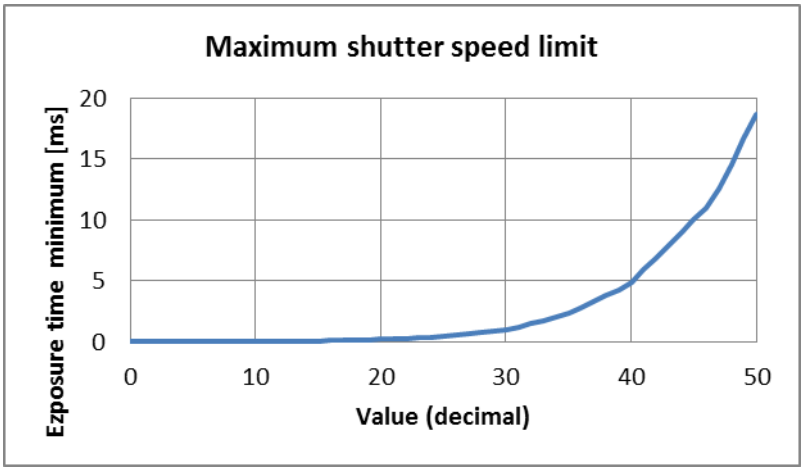
0 = 1/50(PAL) or 1/60(NTSC), which gives a time of 20 or 16,67 milliseconds
1 = 1/100(PAL);1/120(NTSC), which gives a time of 10 or 8,83 milliseconds

Remark: The minimum shutter speed limit is also effective when the shutter speed in the control register is set to Auto.

The lower time boundary can be adjusted with the maximum shutter speed limit.
Bits [6:0] of the value selects the maximum shutter speed limit ranging from 0 to 0x32(50) for PAL or 0 to 0x31(49) for NTSC (see graph)

A value of 0, which is the default, means that the exposure time can decrease until 0,01 milliseconds. A higher value means that the shutter time can't decrease further than that limit.

Next graph shows the relation between the register setting and the minimum exposure time:



Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x05	[7:0]	0x00
Bit[7]: Minimum shutter speed: 0=1/50(PAL);1/60(NTSC); 1=1/100(PAL);1/120(NTSC) Bits[6:0]: Maximum shutter speed: range = 0x00 … 0x32			

8.7 Auto Exposure Target point

The camera has an auto shutter and gain control. These controls make sure that the output of the camera reaches an average level.

This is calculated by the accumulation of all Y-values of the image and take the average from this. This is compared with the Auto Exposure (AEX) target point.

Depending if the camera is still in the shutter range (scene is relative bright) this is achieved by controlling the shutter. If the shutter reached already the max integration time the gain control will take over till it reaches its max value.

Two separate AEX target points can be adjusted. One AEX target point is applied for normal use when BLC is set to Off (see register 0x13), the other AEX target point is applied when BLC is set to On.

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x06	[7:0]	0x30
Auto exposure target point for Normal Use (=BLC Off); range 0x00 … 0xFF			

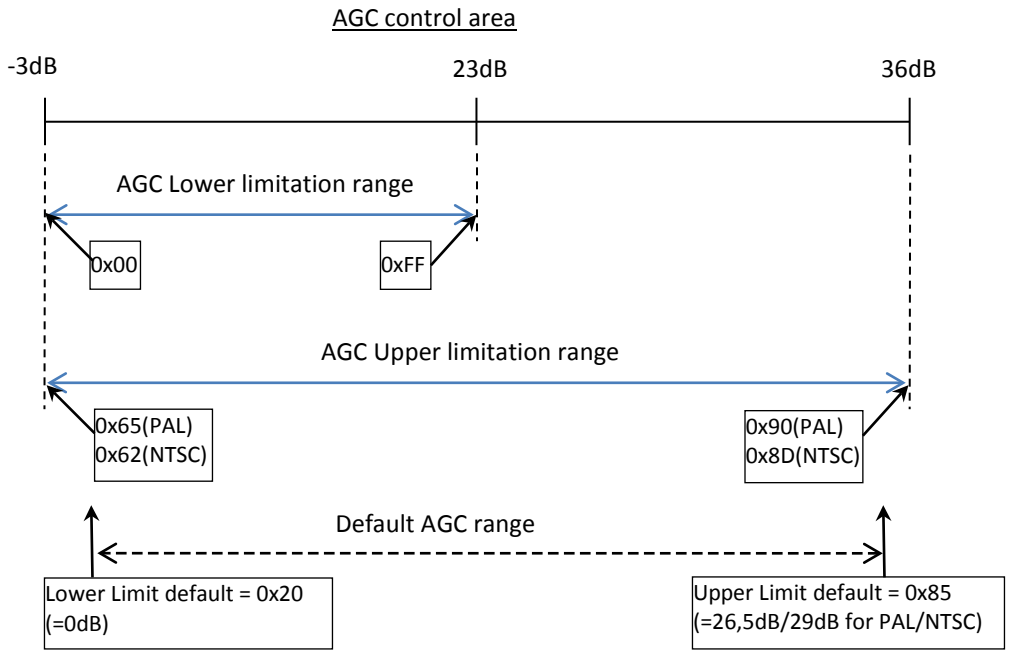
Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x09	[7:0]	0x40
Auto exposure target point when BLC is On; range 0x00 … 0xFF			

8.8 AGC lower and upper Limitation

The camera has automatic gain control in default mode. This function assures that the output signal remains constant at a certain level.

In the exposure control loop when the shutter is at his limit the gain control will take over and assures that the output signal remains constant at a certain level (according the Auto Exposure target point register setting).

Depending on the light conditions the gain amplification factor is automatically adjusted between 0dB up to maximum of 36dB. However you can limit the AGC control area range at the lower and upper side. Refer to the figure below.



The upper limit can be set with the AGC upper Limitation register (register 0x1B). The value can range between 0x65 and 0x90 for PAL and between 0x62 and 0x8D for NTSC. The lowest value sets the gain to 0dB. The highest value set the gain to 36dB.
Note that the upper limit in dB can't be less than the lower limit in dB. This is prevented in the software.

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x1B	[7:0]	0x85
AGC upper limitation value: bit 7:0 (LSB); Valid range 0x65 … 0x90 for PAL and 0x62 … 0x8D for NTSC			

The lower limit can be set with the AGC lower Limitation register. The value can range between 0x00 and 0xFF
(0 = -3dB; 0x20(32) = 0dB; 0x40(32) = 3dB … 0xFF(255) = 23dB).

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x1C	[7:0]	0x20
AGC lower limitation value: bit[7:0]; range 0x00 … 0xFF			

8.9 Back Light Compensation (BLC)

If the register value is 0, it means that the no Back Light Compensation is used and in this case register 0x06 (=Auto exposure target point for Normal Use) determines the AEX target point (=default).

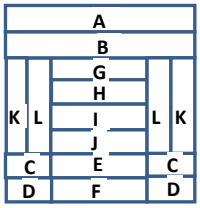
If the register value is > 0, it means that the BLC mode is used and in this case register 0x09 (=Auto exposure target point when BLC is On) determines the AEX target point.

When BLC mode is used, the integrated value for the exposure data of the image is divided into 12 groups (A to L). The coefficients has some prefixed values (register 0x13 = 1, 2 or 3) or can be set individually (register 0x13 = 4).

These coefficients represents weight factors such that groups with a higher value contribute more to the integrated exposure data value.

Next prefixed coefficient list exist:
Register 0x13 = 1: all groups have the same weight of 8.
Register 0x13 = 2: center group have high values; center-off groups lower values.
Register 0x13 = 3: only center groups contribute (BLC= center on).

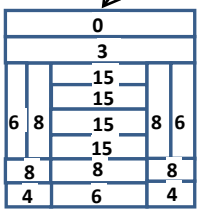
User defined coefficients:
Register 0x13 = 4: use weight factor as set by register 0x9C to 0xA1



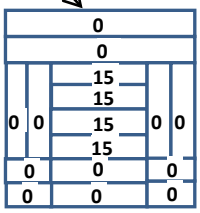
Group	BLC mode register 0x13				
	1	**2**	**3**	**4**	default
A	8	0	0	0x9C[3:0]	6
B	8	3	0	0x9C[7:4]	7
C	8	8	0	0x9D[3:0]	7
D	8	4	0	0x9D[7:4]	6
E	8	8	0	0x9E[3:0]	8
F	8	6	0	0x9E[7:4]	6
G	8	15	15	0x9F[3:0]	11
H	8	15	15	0x9F[7:4]	14
I	8	15	15	0xA0[3:0]	14
J	8	15	15	0xA0[7:4]	11
K	8	6	0	0xA1[3:0]	7
L	8	8	0	0xA1[7:4]	7

evenness settings
(all weight factors are 8)

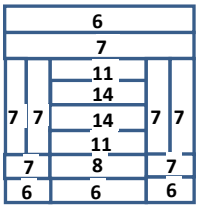
center emphasized



only center



user definable
(defaults)



Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x13	[2:0]	0x00
BLC mode: 0: OFF 1: ON: evenness (all groups the same weight) 2: ON: center emphasized 3: ON: only center 4: ON: user definable (see registers 0x9C .. 0xA1)			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x9C	[7:0]	0x76
Bits[3:0] BLC group A coefficient Bits[7:4] BLC group B coefficient			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x9D	[7:0]	0x67
Bits[3:0] BLC group C coefficient Bits[7:4] BLC group D coefficient			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x9E	[7:0]	0x68
Bits[3:0] BLC group E coefficient Bits[7:4] BLC group F coefficient			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x9F	[7:0]	0xEB
Bits[3:0] BLC group G coefficient Bits[7:4] BLC group H coefficient			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0xA0	[7:0]	0xBE
Bits[3:0] BLC group I coefficient Bits[7:4] BLC group J coefficient			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0xA1	[7:0]	0x77
Bits[3:0] BLC group K coefficient Bits[7:4] BLC group L coefficient			

8.10 White Balance Red and Blue gains

Via the control register the user can select 3 fixed white balance modes: WB1, WB2 and WB3. For each of these setting the corresponding Red and Blue gain can be adjusted.

Note: All white balance gain settings cannot be set in B/W cameras (2xD05x)

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x42	[7:0]	0x68(PAL);0x88(NTSC)
WBR1: White Balance Red Gain (indoor 3200K)			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x43	[7:0]	0x74(PAL);0x70(NTSC)
WBB1: White Balance Blue Gain (indoor 3200K)			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x44	[7:0]	0x7B(PAL);0xA8(NTSC)
WBR2: White Balance Red Gain (fluorescent 4500K)			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x45	[7:0]	0x6C(PAL);0x60(NTSC)
WBB2: White Balance Blue Gain (fluorescent 4500K)			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x46	[7:0]	0x98(PAL);0xC9(NTSC)
WBR3: White Balance Red Gain (outdoor 6400K)			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x47	[7:0]	0x50(PAL);0x4C(NTSC)
WBB3: White Balance Blue Gain (outdoor 6400K)			

8.11 Auto White Balance window

When the Auto White Balance (AWB) is selected in register 0x04, the AWB window can be setup by register 0x34 (window size and window position) setting.

The AWB window contributes to the overall AWB regulation of the image under control of register 0x33 (=weight factor). The weight factor range is between 0 and 64. When the value is 0 (=default value) the entire screen determines the AWB control; when the value is 64, only the AWB window is used.

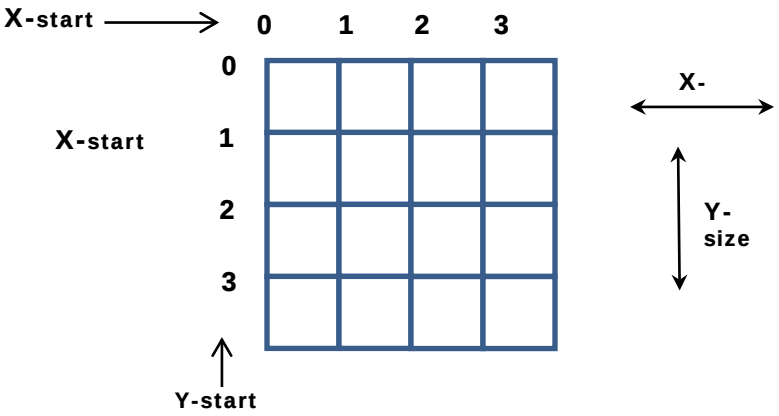
Next equation used for the AWB control is:
((AWB window) * weight_factor + (total screen) * (64 - weight_factor))/64

For the AWB the screen is divided in a 4 x 4 block matrix as illustrated below.
The AWB window is determined by a X- and Y-start coordinate and a X- and Y size.

Both the X- and Y-start positions and the a X- and Y size ranges between 0 and 3 (A value of 0, 1, 2 and 3 means that the AWB size is 1 block, 2 blocks, 3 blocks and 4 blocks respectively).

Register 0x34 control bits are as follows:

- bits 7 and 6 is X-start.
- bits 5 and 4 is Y-start.
- bits 3 and 2 is X-size.
- bits 1 and 0 is Y-size.



Example1:
Reg 0x34 = 0x55
X-pos=1; Y-pos=1; X-size=1; Y-size=1

7	6	5	4	3	2	1	0
0	1	0	1	0	1	0	1

Example2:
Reg 0x34 = 0x69
X-pos=1; Y-pos=2; X-size=2; Y-size=1

7	6	5	4	3	2	1	0
0	1	1	0	1	0	0	1

Note: auto white balance windows cannot be set in black/white cameras (2xD50x)

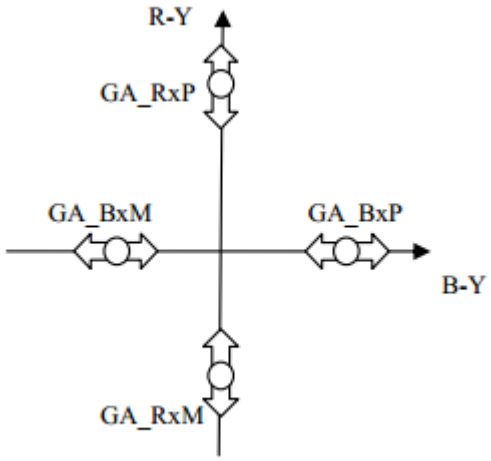
Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x33	[6:0]	0x00
AWB Window weight factor; range 0x00 … 0x40			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x34	[7:0]	0x0F
AWB Position and Size			

8.12 Color Difference Gains

Via the control register the user can select 3 fixed modes: WB1, WB2 and WB3. For each of these 3 setting the 4 corresponding color-difference gains (R-Y negative, B-Y negative, R-Y positive and B-Y positive) can be adjusted.

See figure for the explanation for these gains:



Note: All color difference gains cannot be set in black/white cameras (2xD05x)

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x48	[7:0]	0xA0(PAL);0xA0(NTSC)
WB_R1M: R-Y negative direction color-difference gain (green saturation)			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x49	[7:0]	0xC0(PAL);0xA0(NTSC)
WB_B1M: B-Y negative direction color-difference gain (yellow saturation)			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x4A	[7:0]	0x60(PAL);0x50(NTSC)
WB_R1P: R-Y positive direction color-difference gain (red saturation)			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x4B	[7:0]	0x80(PAL);0x80(NTSC)
WB_B1P: B-Y positive direction color-difference gain (blue saturation)			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x4C	[7:0]	0xD0(PAL);0xD0(NTSC)
WB_R2M: R-Y negative direction color-difference gain (green saturation)			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x4D	[7:0]	0x80(PAL);0x80(NTSC)
WB_B2M: B-Y negative direction color-difference gain (yellow saturation)			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x4E	[7:0]	0x65(PAL);0x65(NTSC)
WB_R2P: R-Y positive direction color-difference gain (red saturation)			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x4F	[7:0]	0x60(PAL);0x60(NTSC)
WB_B2P: B-Y positive direction color-difference gain (blue saturation)			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x50	[7:0]	0xD0(PAL);0xD0(NTSC)
WB_R3M: R-Y negative direction color-difference gain (green saturation)			

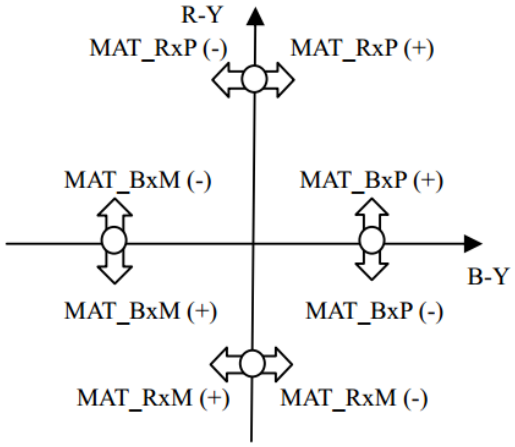
Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x51	[7:0]	0x70(PAL);0x70(NTSC)
WB_B3M: B-Y negative direction color-difference gain (yellow saturation)			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x52	[7:0]	0x80(PAL);0x80(NTSC)
WB_R3P: R-Y positive direction color-difference gain (red saturation)			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x53	[7:0]	0x65(PAL);0x65(NTSC)
WB_B3P: B-Y positive direction color-difference gain (blue saturation)			

8.13 Color Difference Phase Adjustments

Via the control register the user can select 3 fixed modes: WB1, WB2 and WB3. For each of these 3 modes the corresponding phase of the color-difference signal on R-Y and B-Y axis can be adjusted.
See figure for the explanation for these gains:



Note: All color difference phase adjusters cannot be set in black/white cameras (2xD05x)

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x54	[7:0]	0x50(PAL);0x50(NTSC)
MAT_R1M: amount of B-Y correction toward R-Y axis in – region (for WB1)			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x55	[7:0]	0xA0(PAL);0xA0(NTSC)
MAT_B1M: amount of R-Y correction toward B-Y axis in – region (for WB1)			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x56	[7:0]	0x10(PAL);0x10(NTSC)
MAT_R1P: amount of B-Y correction toward R-Y axis in + region (for WB1)			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x57	[7:0]	0x20(PAL);0x20(NTSC)
MAT_B1P: amount of R-Y correction toward B-Y axis in + region (for WB1)			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x58	[7:0]	0x50(PAL);0x50(NTSC)
MAT_R2M: amount of B-Y correction toward R-Y axis in – region (for WB2)			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x59	[7:0]	0xD0(PAL);0xD0(NTSC)
MAT_B2M: amount of R-Y correction toward B-Y axis in – region (for WB2)			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x5A	[7:0]	0x10(PAL);0x10(NTSC)
MAT_R2P: amount of B-Y correction toward R-Y axis in + region (for WB2)			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x5B	[7:0]	0x30(PAL);0x40(NTSC)
MAT_B2P: amount of R-Y correction toward B-Y axis in + region (for WB2)			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x5C	[7:0]	0x00(PAL);0x00(NTSC)
MAT_R3M: amount of B-Y correction toward R-Y axis in – region (for WB3)			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x5D	[7:0]	0xF0(PAL);0xF0(NTSC)
MAT_B3M: amount of R-Y correction toward B-Y axis in – region (for WB3)			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x5E	[7:0]	0x10(PAL);0x10(NTSC)
MAT_R3P: amount of B-Y correction toward R-Y axis in + region (for WB3)			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x5F	[7:0]	0x20(PAL);0x20(NTSC)
MAT_B3P: amount of R-Y correction toward B-Y axis in + region (for WB3)			

8.14 Day/night functionality

The camera is equipped with a day/night function that can automatically switch from color to black/white when light conditions deteriorate. The switch from color to black/white is done to reduce color noise introduced by an increasing AGC gain. This function only works when the AGC is not in fixed mode.

Note: Day/Night mode is standard in "Black/white without color burst" mode for black/white camera's and cannot be altered.

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x60	[1:0]	0x03
00: Black/white without colorburst (normal B/W mode) 10: Black/white with colorburst 01: Color 11: Day/night (automatic mode)			

In automatic mode the camera determines the moment it switches from day to night mode according to the amount of AGC gain applied to the image. To prevent day/night oscillation the following condition has to be met:

- day_night_threshold > night_day_threshold

Also make sure the AGC_upper_limitation is set to a sufficient level otherwise the function might not function as desired.

Device address	Register address	Bits	Default value
0x30/0x31 (w/r)	0x62	[7:0]	0x80
day_night_threshold; range: 0x62 – 0x90			

In automatic mode the camera determines the moment it switches from night to day mode according to the amount of AGC gain applied to the image. To prevent day/night oscillation the following condition has to be met:

- day_night_threshold > night_daythreshold

Device address	Register address	Bits	Default value
0x30/0x31 (w/r)	0x63	[7:0]	0x70
night_day_threshold; range: 0x62 – 0x90			

In addition to the threshold values a switching delay can be applied. This delay is useful when light conditions vary for a few seconds and an output switch is not desirable for these few seconds. The delay time can be calculated according to the following formula:

$$t_{seconds} = \frac{2^X}{F}$$

t = delay time in seconds
X = value in register nibble (0 – 15)
F = Analog output frequency (50Hz for PAL and 60Hz for NTSC)

For convenience a look-up table with approximated values is supplied:

Value	Delay [fields]	Time for PAL [seconds]	Time for NTSC [seconds]
0	1	0.02	0.02
1	2	0.04	0.03
2	4	0.08	0.07
3	8	0.2	0.1
4	16	0.3	0.3
5	32	0.6	0.5
6	64	1.3	1.0
7	128	2.6	2.1
8	256	5.1	4.3
9	512	10	8.5
A	1024	21	17
B	2048	41	34
C	4096	81 (1.4 minutes)	66 (1.1 minutes)
D	8192	163 (2.7 minutes)	138 (2.3 minutes)
E	16384	327 (5.5 minutes)	276 (4.6 minutes)
F	32768	655 (10.9 minutes)	546 (9.1 minutes)

Device address	Register address	Bits	Default value
0x30/0x31 (w/r)	0x64	[7:0]	0x55
Bit[3:0]: night_day_delay; range: 0x0 – 0xF Bit[7:4]: day_night_delay; range: 0x0 – 0xF			

8.15 Edge Enhancement / Sharpness

Edge enhancement will increase the sharpness impression of the camera. Both the horizontal and vertical level can be set separately and can even be switched off.

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x7B	[1:0]	0xD0
Bit[0]: Horizontal edge enhancement On/Off; 0 = ON; 1 = OFF Bit[1]: Vertical edge enhancement On/Off; 0 = ON; 1 = OFF			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x7C	[4:0]	0x17 (2xK17x) 0x09 (2xD17x) 0x10 (2xD0xx)
Horizontal edge enhancement gain; range 0x00 … 0x1F			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x7E	[4:0]	0x17 (2xK17x) 0x09 (2xD17x) 0x10 (2xD0xx)
Vertical edge enhancement gain; range 0x00 … 0x1F			

8.16 Blemish Correction

The camera is equipped with an automatic blemish detection and compensation circuit, which can correct a maximum of 8 white pixels.

Before starting the automatic blemish correction process, the lens must be totally covered to avoid that incident light strikes the sensor.

Start the process with the START command written to the register address, next the screen will turn to blue. Wait approximately 5 seconds until the process has finished and when successful the “white” pixels should be vanished.

During the blemish correction process no I^2C communication with the camera is possible.

Afterwards you can read the result of the process with a read from the register address. The value indicates whether the process was failed or successful. Also it indicates and how many pixels are corrected in case of success.

With a CLEAR command you can clear all corrected pixels (so the “white” pixels appear again).

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x81	[7:0]	0x00
Write: Value = 1: START blemish correction and apply it. Value = 2: CLEAR all blemish corrected pixels			
READ: Bits[3:0]: Result: 0 = SUCCESS; ≠ 0 = FAILED Bits[7:4]: Number of corrected pixels (range 0 to 8)			

When the standard blemish correction setting does not provide the satisfied result the sensitivity may be adjusted. A higher value corrects larger blemishes first and a lower value corrects smaller blemishes first.

Note: A low blemish correction level may correct noise pixels and therefore create flashing pixels.

Device address	Register address	Bits	Default value
0x30/0x31 (w/r)	0x80	[7:0]	0x10
Bit[7:0]: Blemish correction sensitivity. Range: 0x20 – 0x08			

8.17 High luminance color suppression start level

The high luminance color suppression turns high intensity colors white to prevent a color change to white objects. However, when set too low the dynamic range of the sensor is compromised. But when set too high white objects may appear blue/purple in bright light conditions.

Note: Color settings cannot be modified for black/white cameras (2xD05x)

Device address	Register address	Bits	Default value
0x30/0x31 (w/r)	0xA6	[7:0]	0xC0 (2xK17x) 0x80 (2xDxxx)
Bit[7:0]: High luminance color suppression start level			

8.18 Color edge suppression gain

When a high contrast transition is within the image some artifacts may appear in the image. To decrease this effect a color edge suppression filter can be used.

However, this filter can add color clipping as a side effect. For maximum enhancement of the picture it is possible to adjust this gain level.

Note: Color settings cannot be modified for black/white cameras (2xD05x)

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0xA7	[7:0]	0x99 (2xK17x) 0x00 (2xDxxx)
Bit[3:0]: Vertical edge color suppression gain (positive number) Bit[7:4]: Horizontal edge color suppression gain (positive number)			

8.19 Digital Output

The digital output CLKOUT and DOUT7 to DOUT0 can be enabled or disabled. Beside the CLKOUT polarity can changed.

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x82	[1:0]	0x00
Bit[0]: Digital output: 0 = enabled; 1 = disabled Bit[1]: CLKOUT polarity: 0 = normal (DOUT changed on falling edge); 1 = inverse (DOUT changed on rising edge);			

The digital output luminance and chrominance gain can be set individually.

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x83	[7:0]	0x78
Digital Luminance gain: range 0x00 … 0xFF			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x84	[7:0]	0x6C
Digital Chrominance gain: range 0x00 … 0xFF			

8.20 Analog Output

The analog CVBS output signal can be parametrized with the following settings:

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x88	[1:0]	0x15
CVBS Setup Level (two's complement); 0x15 = 50 millivolt.			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x89	[7:0]	0x2E
Bits[6:0]: CVBS Burst Level R-Y Bit[7]: 1 = -direction; 0 = +direction			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x8A	[7:0]	0x2A
Bits[6:0]: CVBS Burst Level B-Y Bit[7]: 1 = -direction; 0 = +direction			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x8B	[4:0]	0x10
CVBS Analog Output gain (1x at 0x10)			

Device address	Register address	bits	Default value
0x30/0x31 (w/r)	0x8C	[7:0]	0x75
CVBS Sync Level Adjustment			

8.21 EEPROM Save Register commands

With this register one can give one of possible two commands:

1) Save the current settings in the EEPROM (in page 0).
2) Initialize the camera to the factory defaults (EEPRPM page 2 is copied to EEPROM page 0).

After this command is issued, wait for 2 seconds, then repower the camera, the camera will start up with the default settings.

Device address	Register address	bits	Write Only
0x30/0x31 (w)	0xf0	[7: 0]	--
Value = 1: Save current settings in user setting area (= EEPROM page 0). This means that after a repower, settings will be the same. Value = 2: Set default settings in user setting area (=EEPROM page0): This means that the factory settings in EEPROM page 2 is copied to EEPROM page 0. Remark: all other values are rejected			

8.22 Password

A 2 bytes password is used to avoid that accidental addressing of ISP registers is applied. Both number must be filled before access to ISP registers is granted.

Device address	Register address	bits	Default value
0x30/0x31 (write)	0xfc	[7: 0]	0x00
MSB password			

Device address	Register address	bits	Default value
0x30/0x31 (write)	0xfd	[7: 0]	0x00
LSB password			

8.23 Micro Software Version

Device address	Register address	bits	Read only
0x30/0x31 (r)	0xff	[7: 0]	0x10
Software Version of the Microcontroller Bits[7:4]: Major number; Bits[3:0]: Minor number. example: Data=0x13 means V1.3 (1=major, 3=minor)			

9 Access control

Write access to the EEPROM page 0 in the range 0x00 to 0xF7 and the entire EEPROM page 1 is permitted. However the remaining locations 0xF8 to 0xFF of EEPROM page 0 and all EEPROM page 2 and 3 registers are write protected.

Also read and write access to the DSP registers and ISP EEPROM pages (mode value = 0x80/0x81) are protected.

The protection can be disabled when the correct password values are written into the camera registers 0xfc and 0xfd.

10 USB-I²C interface tool

Videology also offers hardware to control the camera via I²C as well as a software control application.

To control the camera via the PC an I²C-USB interface board is available. The type number of the board is 72V0070. This board is part of the cable kit to connect that board (type number 60K5-U).

10.1 I²C Board Connections

!IMPORTANT!

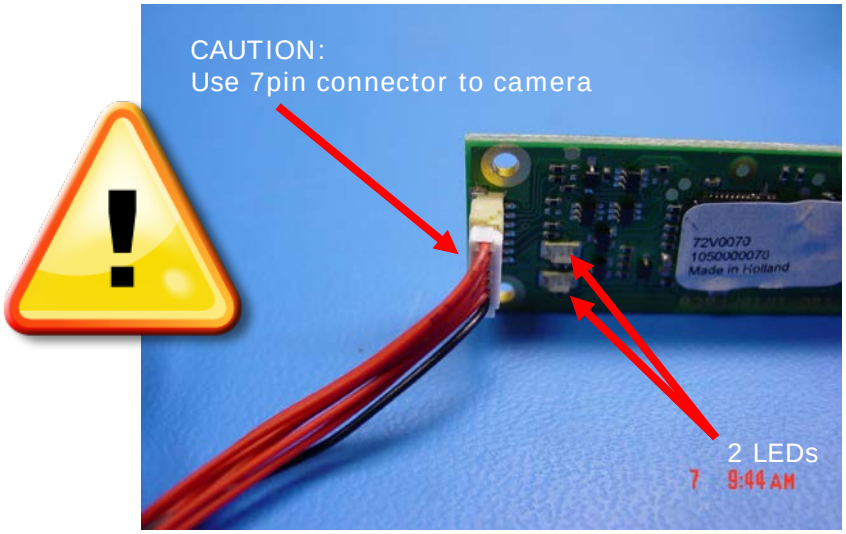
60C1045	7pin cable (connects to camera, 2 LEDs side of I²C board)
60C1062	6pin cable (connects to computer, 1 LED side of I²C board)

Using these figures as reference, follow the steps outlined below:

- Lay out the Camera, USB-I²C interface board (72V0070), computer and monitor on your work area
- Locate the 72V0070 USB to I²C Interface board

- Connect the 7pin 60C1045 cable to the USB-I²C interface board

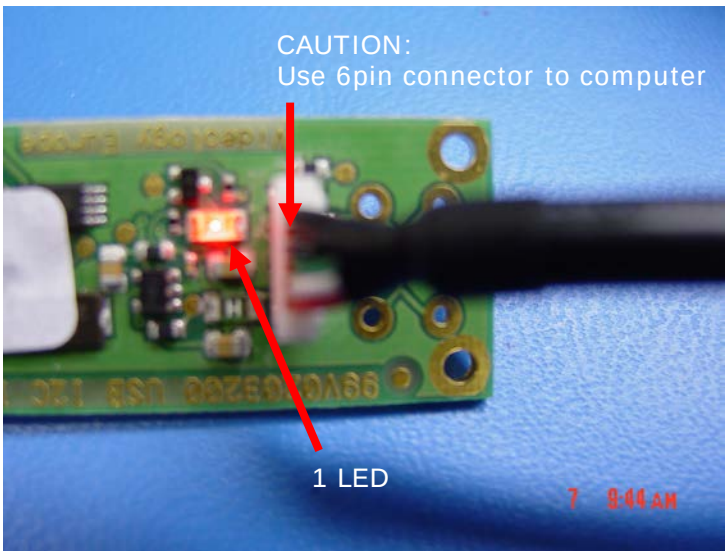
  CAUTION: ensure you are **not** using the **6pin** 60c1062 cable for this connector!
  Damage to USB camera may occur!



The top LED will flicker when choosing commands

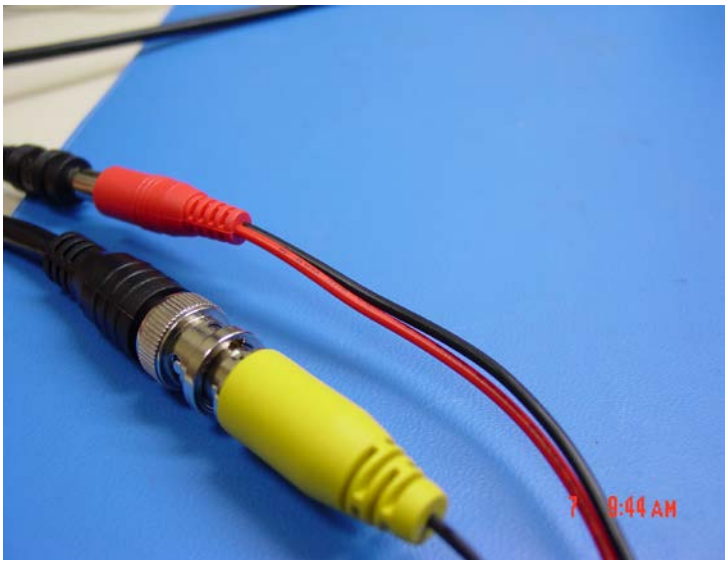
The Second LED will stay on when there is an error

- Connect the 6pin 60C1062 cable to the USB-I²C interface board
  DO NOT CONNECT THIS TO THE PC YET…



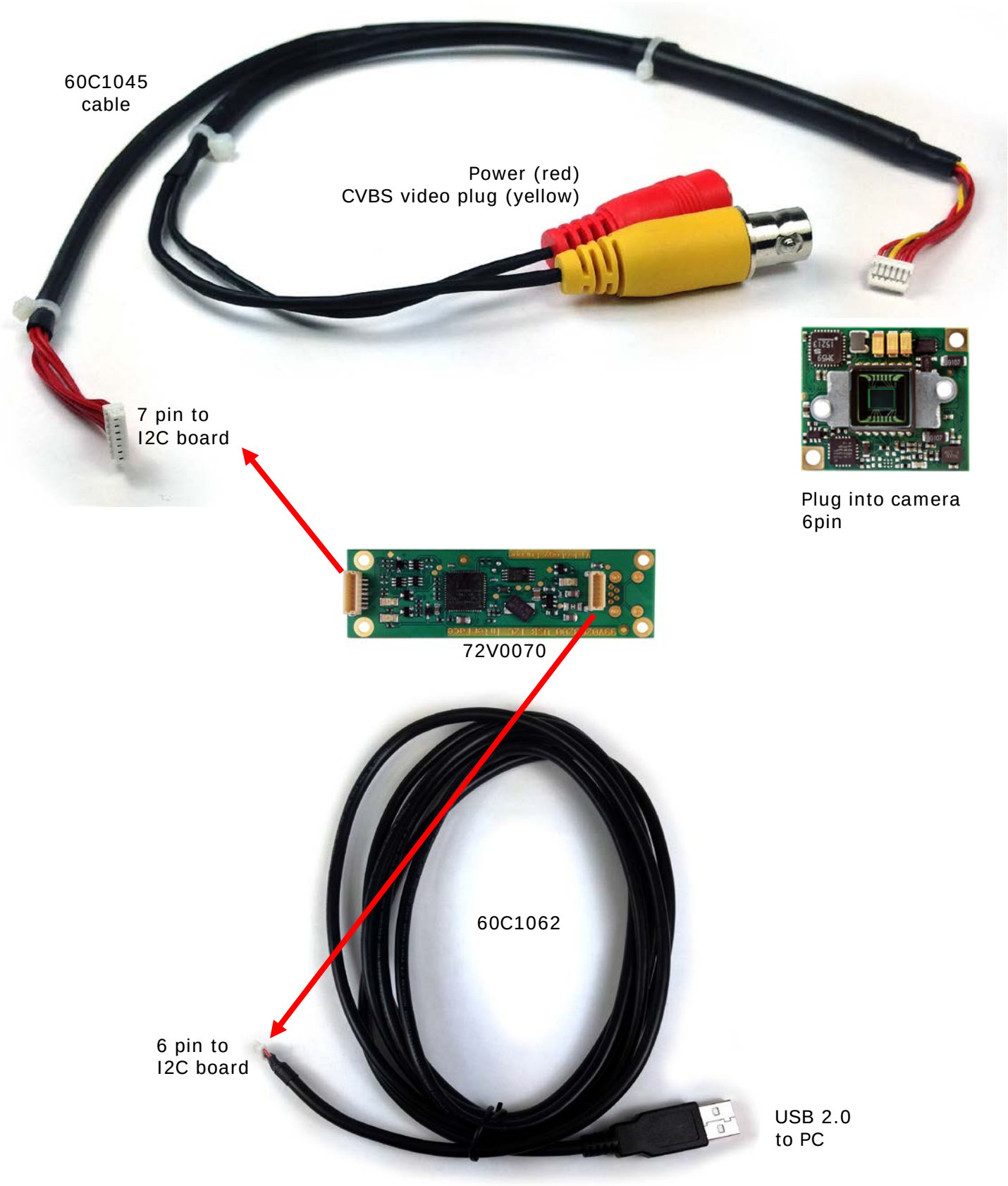
LED is on when USB cable is connected

- Connect the 5VDC power supply to the 60C1045 cable
- Connect the BNC to BNC cable to the monitor and to the 60C1045 cable



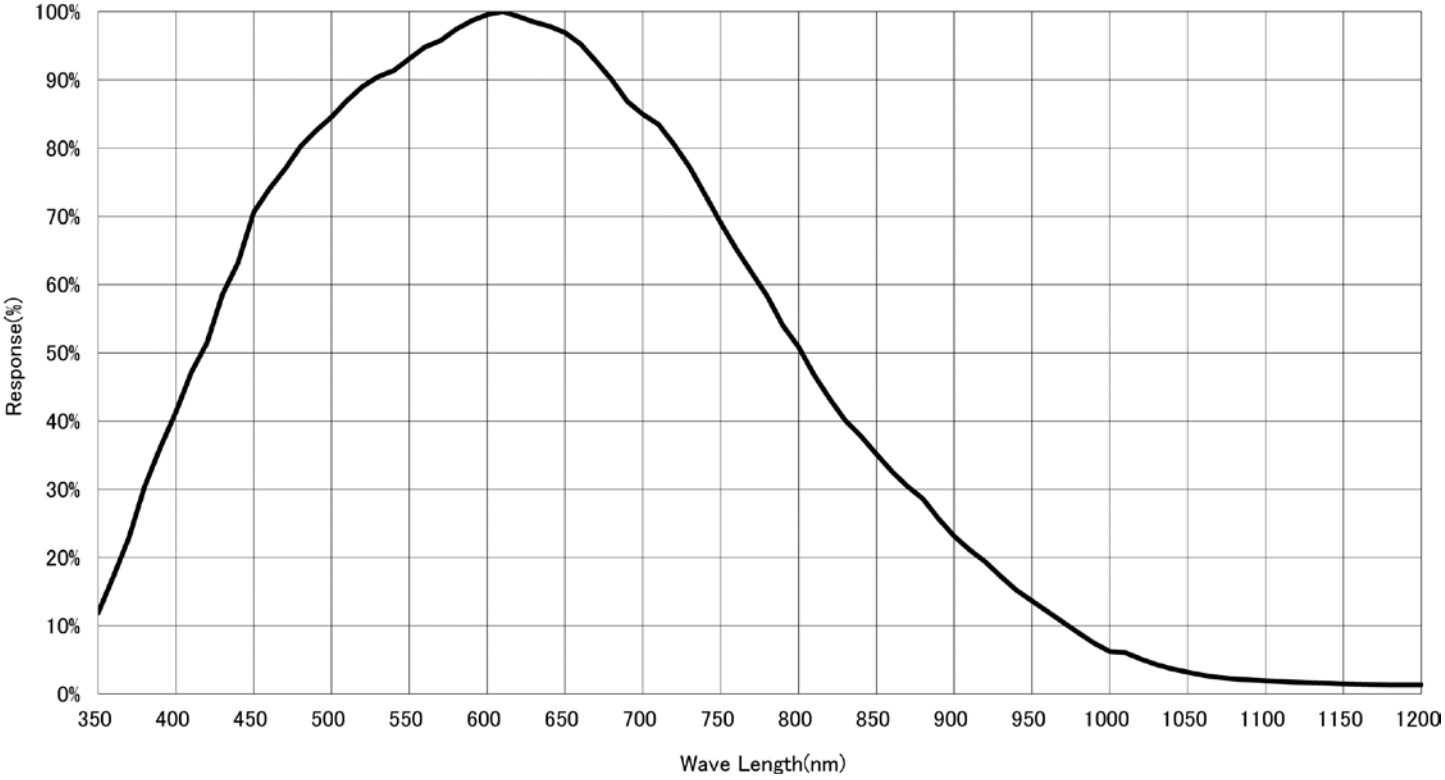
10.2 I²C Board Connection Layout

!IMPORTANT!



11 Spectral Response

2xD05X camera



12 Application Software

Videology can provide also software tools to control the camera. Please contact us for more information.

13 Contact Information

For technical assistance with this product, please contact the supplier from whom the product was purchased.

For OEM inquiries, contact Videology® Imaging Solutions:

Americas, Middle East, Far East & Australia:
Videology® Imaging Solutions Inc.
37M Lark Industrial Parkway
Greenville, RI 02828
USA

Tel: (401) 949-5332
Fax: (401) 949-5276

Europe & N. Eurasia:
Videology® Imaging Solutions Europe B.V.
Neutronenlaan 4
5405 NH Uden
The Netherlands

Tel: +31 (0) 413-256261
Fax: +31 (0) 413-251712

Please visit our website: videologyinc.com

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