VIDEOLOGY®

IMAGING SOLUTIONS INC.

Application Note

20/21K13XDIG (B&W)
20/21K14XDIG (Color)
20/21K15XDIG (Color)

Information may change without notice.

This document provides technical information for the user. Videology reserves the right to modify the information in this document as necessary. The customer should make sure that they have the most recent manual version. Videology holds no responsibility for any errors that may appear in this document.

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1 Introduction

The 20/21K13XDIG, 20/21K14XDIG, and 20/21K15XDIG cameras are based on the standard 20/21K13X, 20/21K14X, and 20/21K15X respectively. It is mechanically identical, having a 1/4" CCD, and identical dimensions (22x26mm) and mounting holes. The "DIG" versions are equipped with digital output, which is described fully in this document. The camera can be operated via a 17-pole flex-foil connector or with the 30-pin board-to-board connector. This 30-pin board-to-board connector can be used to "piggy-back" an application PCB.

An example of an Application PCB is:

- USB 2.0 Board: Videology product that has same dimensions (22x26mm). When two boards are stacked together a complete USB 2.0 camera is available.
- Ethernet interface (not yet available)
- 12VDC to 5VDC power conversion board with audio option (Models 20/21K145VDN).
- 24VAC/12VDC power board with DC auto iris and isolation transformer (Model 60PB24VB).

This document is written to give technical background on specific features of these cameras.

2 History

Revision	Issue date	Reason
Rev 0	07/09/04	Initial
Rev A	07/13/04	Format adaptation
Rev B	04/08/04	Update
Rev C	12/08/04	Add connector positions
Rev D	28/09/04	Changed digital format timing
Rev E	03/14/05	Reformat
Rev F	05/12/05	Change VD pulse to "negative going polarity" p.17
Rev G	10/26/05	Update, Added 20K13XDIG, Appendix Compatible ICS
Rev H	08/21/06	3 features, 5.4 BLC
Rev I	03/27/08	Section 10.1.2 20/21K13XDIG pins 19 & 20 swapped

3 Features:

3.1 Standard Resolution Version (color) – 20/21K14XDIG

20K14XDIG (**NTSC**) **/ 21K14XDIG** (**PAL**)

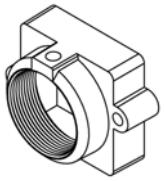
Standard basic features:

	20K14XDIG (**NTSC**)	**21K14XDIG** (**PAL**)
CCD sensor	1/4" IL CCD	
Active pixels (HxV)	510 x 494 NTSC	500 x 582 PAL
Horizontal resolution	≥330 TVL	
Sensitivity	< 0.5 Lux (50 IRE) F1.2 3200K, lens transmission 80%, scene reflection 75%	
	.05 lux in night mode* (20K14XDN)	
Signal to noise ratio	> 52 dB analog output 48 dB (AGC off) digital output	
Gamma	0.45 default (1.0 via Software)	
Gain control	Automatic 36 dB (AGC default) or Fixed options via software	
Scan mode	Interlaced / Non Interlaced (selectable via Software)	
Mirror mode	Selectable via software	
Synchronization	Internal	
Back light compensation	Default on (selectable via software)	
White balance mode	AWB auto white mode, Fixed modes selectable via software	
Contour enhancement	Default on	
Iris control	CCD Iris default	
Shutter speeds	Automatic from 1/60 to 1/100,000	Automatic from 1/50 to 1/100,000
	14 fixed speeds via software	
Video output	- 8-bit digital YUV 4:2:2 @ CCIR656, CMOS output, 3.3V level - 16-bit digital output CCIR601, CMOS Output, 3.3V Level	
	Video: Composite 1Vp-p CVBS (75 ohms)	
Control communication	I²C control	
Power supply	5VDC ± 5% (not polarity protected)	
Power consumption	< 0.8 W	

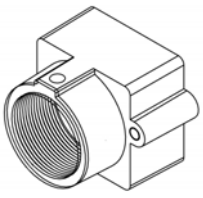
Lens Mounts:
Replace "X" in model number with desired lens mount option:

Example: Change 20K14**X**DIG To 20K14**5**DIG To Select An M-12 Board Mount.

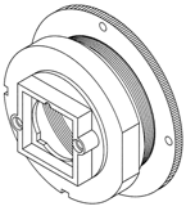
20K14**2**DIG
Pinhole lens



20K14**5**DIG
Board lens (M12 lens)



20K14**8**DIG
C/CS-mount version



Software to control the camera is available upon request.

3.2 High Resolution Version (color) – 20/21K15XDIG

20K15XDIG (NTSC) / 21K15XDIG (PAL)

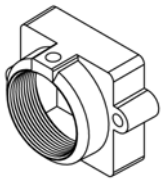
Standard basic features:

	20K15XDIG (NTSC)	**21K15XDIG (PAL)**
CCD Sensor	1/4" IL CCD	
Active pixels (HxV)	768 x 494	752 x 582
Horizontal resolution	>460 TVL	
Sensitivity	< 1.0 Lux	
Signal to noise ratio	> 52 dB analog output 48 dB (AGC off) digital output	
Gamma	0.45 default (1.0 via Software)	
Gain Control	Automatic 36 dB (AGC default) or fixed options via software	
Scan Mode	Interlaced / Non Interlaced (selectable via software)	
Mirror Mode	Selectable via software	
Synchronization	Internal	
Back light compensation	Default on (selectable via software)	
White Balance Mode	AWB auto white mode, fixed modes selectable via software	
Contour enhancement	Default on	
Iris Control	CCD Iris default	
Shutter Speeds	Automatic from 1/60 to 1/100,000	Automatic from 1/50 to 1/100,000
	14 fixed speeds via software	
Video output	- 8-bit digital YUV 4:2:2 @CCIR656, CMOS output, 3.3V level - 16-bit digital output CCIR601, CMOS Output, 3.3V Level Video: Composite 1Vp-p CVBS (75 ohms)	
Control communication	I²C control	
Power supply	5VDC ± 5% (not polarity protected)	
Power consumption	< 0.8 W	

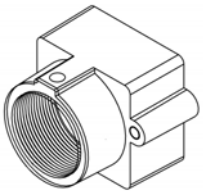
Lens Mounts:
Replace "X" in model number with desired lens mount option:

Example: Change 20K15**X**DIG To 20K15**5**DIG To Select An M-12 Board Mount.

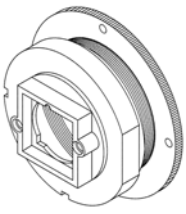
20K15**2**DIG
Pinhole lens



20K15**5**DIG
Board lens (M12 lens)



20K15**8**DIG
C/CS-mount version



Software to control the camera is available upon request.

3.3 High Resolution Version (B&W) – 20/21K13XDIG

20K13XDIG (NTSC) / 21K13XDIG (PAL)

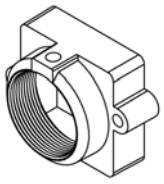
Standard basic features:

	20K13XDIG (NTSC)	**21K13XDIG (PAL)**
CCD Sensor	Sony® 1/4" Ex-View® CCD	
Active pixels (HxV)	768 x 494	752 x 582
Horizontal resolution	≥570 TVL	
Sensitivity	< 0.005 Lux, near IR sensitive	
Signal to noise ratio	> 52 dB analog output 48 dB (AGC off) digital output	
Gamma	0.45 default (1.0 via Software)	
Gain Control	Automatic 36 dB (AGC default) or fixed options via software	
Scan Mode	Interlaced / Non Interlaced (selectable via software)	
Mirror Mode	Selectable via software	
Synchronization	Internal	
Back light compensation	Default on (selectable via software)	
White Balance Mode	AWB auto white mode, fixed modes selectable via software	
Contour enhancement	Default on	
Iris Control	CCD Iris default	
Shutter Speeds	Automatic from 1/60 to 1/100,000	Automatic from 1/50 to 1/100,000
	14 fixed speeds via software	
Video output	- 8-bit digital Y - 16-bit digital output CCIR601, CMOS Output, 3.3V Level Video: Composite 1Vp-p CVBS (75 ohms)	
Control communication	I²C control	
Power supply	5VDC ± 5% (not polarity protected)	
Power consumption	< 0.8 W	

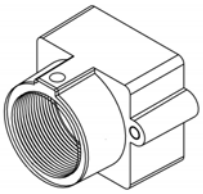
Lens Mounts:
Replace "X" in model number with desired lens mount option:

Example: Change 20K13**X**DIG To 20K13**5**DIG To Select An M-12 Board Mount.

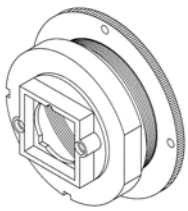
20K13**2**DIG
Pinhole lens



20K13**5**DIG
Board lens (M12 lens)



20K13**8**DIG
C/CS-mount version



Software to control the camera is available upon request.

4 Block Diagram

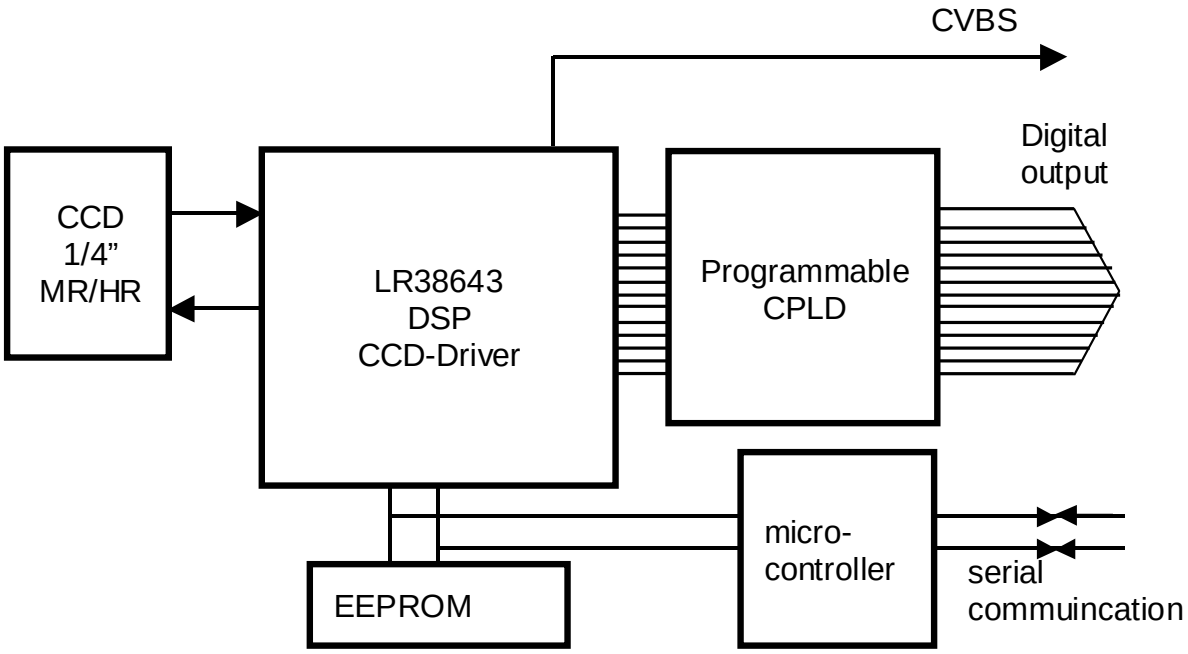


Figure 1. Block Diagram

5 Basic Functions Programmable Via Software:

5.1 White Balance (color models only)

Via software users can select 3 fixed modes or the Auto White balance mode. Select the white-balance mode with bit 0 and bit 1 from register 0x04h. See also table 1 (section 6-1).

5.2 Shutter Speeds

In default mode, the camera operates in the electronic iris mode. This means the CCD output, which is dependent on the light intensity, is controlled by the electronics of the camera and not the mechanics of the lens.

By measuring the output of the CCD and comparing it with an internal reference it is possible to control the level of the signal out of the CCD (within a certain tolerance).

However, users may in some instances prefer that the shutter is fixed and not automatic. For example, a fixed shutter is beneficial is if there is a very fast moving object in the scene. The longer the integration time (the period that no OFD pulse occurs, max 1/50 sec for PAL and max 1/60 sec for NTSC) the less clear the image will appear due to movement of the object during the integration period. To prevent this from occurring the camera has 8 fixed shutter speeds (see table 1 in section 6-1).
The shutter can be set by register 0x04 (bit 6, 5, 4 and 3).

5.3 Mirror Mode

The readout direction can be changed so that the picture is mirrored.
The mirror mode can be set by register 0x04 (bit 7).

5.4 Back Light Compensation (BLC)

The camera has a default setting of standard back light compensation (BLC) ***OFF***. When ***ON***, only the central part of the scene is referenced to determine the level of the CCD output (see figure 2). When fixed shutter speeds are used this function has no effect. If a situation requires that the complete image be used to determine the CCD output level, this can be adjusted via register 0x04h bit 2.

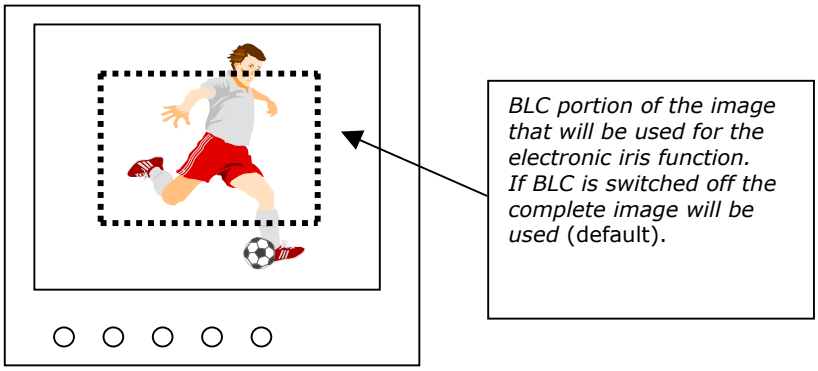


Figure 2. Back Light Compensation (BLC)

5.5 Description Control Register 0x04

5.5.1 20/21K14XDIG 20/21K15XDIG (color) 20/21K13XDIG (B&W)

Note that WB-modes are not active for the 20/21K13XDIG (B&W)

White Balance, Shutter Speed, BLC and Mirror Setting		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Mode	Red gain address WBR	Blue gain address WBB
Mirror mode active		1	X	X	X	X	X	X	X			
BLC active		X	X	X	X	X	1	X	X			
WB-mode 1		X	X	X	X	X	X	0	1	Indoor 3200K	0x42	0x43
WB-mode 2		X	X	X	X	X	X	1	0	Fluorescent 4500K	0x44	0x45
WB-mode 3		X	X	X	X	X	X	1	1	Outdoor 6400K	0x46	0x47
Auto White Balance		X	X	X	X	X	X	0	0	auto	auto	auto
Shutter Speed:												
PAL	NTSC											
1/50	1/60	X	0	0	0	0	X	X	X			
1/120	1/100	X	0	0	0	1	X	X	X	Flickerless mode		
1/250		X	0	0	1	0	X	X	X			
1/500		X	0	0	1	1	X	X	X			
1/1,000		X	0	1	0	0	X	X	X			
1/2,000		X	0	1	0	1	X	X	X			
1/5,000		X	0	1	1	0	X	X	X			
1/10,000		X	0	1	1	1	X	X	X			
1/20,000		X	1	0	0	0	X	X	X			
1/50,000		X	1	0	0	1	X	X	X			
1/100,000		X	1	0	1	0	X	X	X			
PAL	NTSC											
1/25	1/30	X	1	0	1	1	X	X	X	See note		
1/12.5	1/15	X	1	1	0	0	X	X	X	See note		
1/6.25	1/7.5	X	1	1	0	1	X	X	X	See note		
Auto		X	1	1	1	0	X	X	X	1/50 or 1/60 to maximum shutter speed setting in register address 0x05		
Auto		X	1	1	1	1	X	X	X	1/50 or 1/60 to 1/100,000		

Note: Frame-storage for capturing is necessary.

5.6 AGC

The camera has an automatic gain control in default mode. This function assures that the output signal remains constant at a certain level. If the camera is pointed to a gamma reflection chart 0.45 the output should be 1Vp-p. This control circuit works with an integrator. The integrator generates from the video signal, which is a signal that corresponds with the average value of the video signal. This average is compared with an internal reference and depending on the outcome of the gain will increase or decrease.

5.7 Manual Gain Control

If the automatic gain control is switched off, set register 0x02h bit 1 to **1** (when bit 1 is 0, the gain is auto). To set the manual gain the user should write a value to register 0x1Dh (00 is minimum, FF is maximum) to obtain the maximum range. Also, bit 8 should be set (AGC range is 9 bit). This can be done in register 0x1e: set bit 3 to 1.

5.8 Gamma

Gamma function corrects the non-linear behavior of the CRT monitor. The gamma curve of the camera is 0.45. With this gamma setting the monitor is able to display the scene as we see it with our eyes.

However, if the camera video signal is processed for pattern recognition this gamma function may not be desirable. To make this adjustment, the 20/21K14x has a gamma option that can be selected via the software serial interface. See software-appendix with more details on DSP – settings.

5.9 Interlacing

The camera normally runs in the interlaced mode according to the PAL or NTSC standard. This means that a full picture (frame) is built up out of two half pictures (fields) which are shifted half a line and referenced to each other. For a graphical view see figure 3.

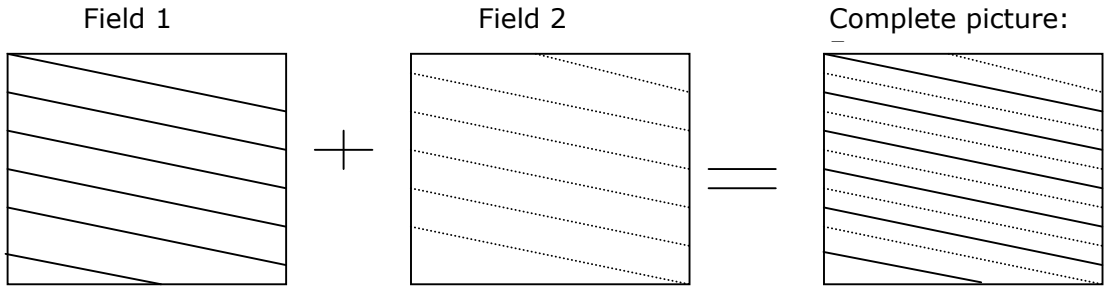


Figure 3. Interlaced Display

This means that every 40ms (for PAL) or 33.3ms (for NTSC) the camera generates a complete picture.

However, sometimes the application does not require high vertical resolution, but must still have the same information from each field (without the half line shift between the fields). In that case, the two fields are identical to each other. See figure 4 (section 5).

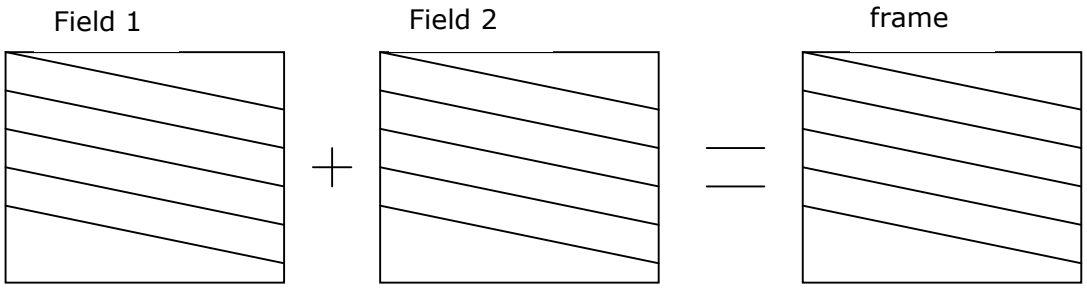


Figure 4. Non-Interlaced Display

In figure 4 it can be seen that the vertical resolution is less compared to the interlaced mode (see figure 3), but that the fields are identical with each other and therefore the frame rate is increased (doubled).

To put the camera in the non-interlaced mode change bit 6 to **1** of register 0x02h.

5.10 Frame Rate

20/21K14XDIG 20/21K15XDIG (color)
The camera's normal operation is according to the NTSC (60Hz) or PAL (50Hz) standard. However the components are selected in such a way that by increasing the main clock frequency, the vertical frequency can be increased up to 75 Hz.

20/21K13XDIG (B&W)
The camera's normal operation is according to the EIA or CCIR standard. However the components are selected in such a way that by increasing the main clock frequency, the vertical frequency can be increased up to 75 Hz. Ask Videology for more info.

5.11 Outputs

- Digital CCIR656 8 bits YUV 4:2:2. In case of the 20/21K13XDIG versions the U and V is always set to 0x80 (which is equal to zero. Digital CCIR601 16 bits Y and UV data (only for color version 20/21K14XDIG & 20/21K15XDIG, only via board-to-board connector)
- Analog CVBS output (only via board-to-board connector)

6 Software Control

The camera has a serial control interface via three wires:

- Data wire
- Clock wire
- Ground wire

This interface operates similar as to the I^2C-protocol.
Data, address and registers are all 8-bit words. The graphic interface is shown in figure 5. The maximum speed limitation is 10kHz. The minimum speed should be higher than 100Hz.

The write action to the EEPROM needs to be done with a delay time between the write actions of at least 10msec.

A wait time is further required between commands, so that the internal communication has the time to make the required internal communication. The delay time between the commands should be at least 2msec.

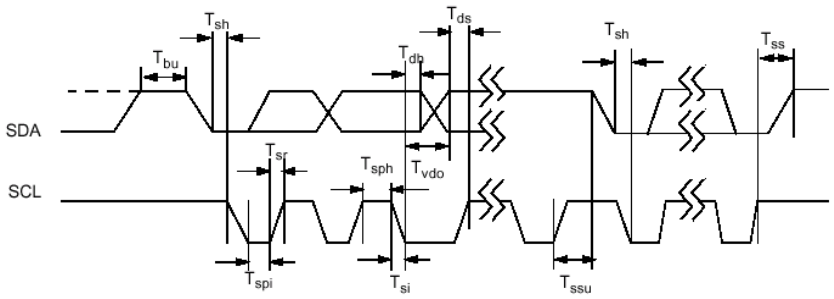


Figure 5. Communication Timing

Standard I^2C address camera: 0x70
The communication-structure contains a Command block and a Data block.

Command block:

<START> <cam_address>ackn<acces_mode>ackn<device>ackn <register>ackn<STOP>

Cam_address	Acces_mode	device
Standard=0x70*	00=write to camera 01=read to camera	00=encoder 30=DSP a0,a2,a4,a6= EEPROM

*A new I^2C address can be added. The camera's address is stored in address 0x90 of the EEPROM (page 2: 0xa2/0xa3). The camera can be given a new address if the user wishes to do so. Default address 70 will always be active, but users can give a second address where the camera reacts. If the second address is forgotten, the user can revert to the default address.

Data block:

<START><cam_addressR/W>ack<data>ackn/Nackn***<STOP>**

Cam_address	**Data:**
Access mode=00: 0x70 Access mode=01: 0x71	Write data to camera with ***ackn***. Read data from camera with ***Nackn.*****

**NOT acknowledge means: master sends a clock *low high low* as with a normal acknowledge, but the camera may not respond by pulling data line low. This must be checked, or the number of bits will not be correct!

Example 1. Write Action:
Set shutter speed to 1/250 seconds, this means:
Write DSP 30 register 04 and data 80 (see shutter speed-table 1):

Write action:
Command-block:
<start> 70 ackn 00 ackn 30 ackn 04 ackn <stop>
datablock:
<start> 70 ackn 80 ackn description: camera-address 70, access mode write, device 30 (DSP), register 04,
datablock: write address 70 , data 80.

To save value in the EEPROM:
Write EEPROM page 1 A0 register 04 and data 80
Write action:
Command-block:
<start> 70 ackn 00 ackn A0 ackn 04 ackn <stop>
datablock:
<start> 70 ackn 80 ackn
description: camera-address 70, access mode write, device A0 (Write page 1 eeprom), register 04,
datablock: write address 70 , data 80.
Example 2 Read action: EEPROM page 1; register 04 and read data:

Read action:
Command-block:
<start> 70 ackn 01 ackn A1 ackn 04 ackn <stop>
datablock:
<start> 71 ackn Nackn
description: camera-address 70, access mode read, device A1 (eeprom page 1 read), register 04,
datablock: read address 71 , camera will sent data.

6.1 Camera Configuration:

The device addresses have two values; one for read, and one for write. The difference is that the last bit (LSB) is set to ***1***. For communication, the following device addresses are available:

Device	Device write	Device read
DSP	0x30	Not possible
EEPROM page 1	0xa0	0xa1
EEPROM page 2	0xa2	0xa3
EEPROM page 3	0xa4	0xa5
EEPROM page 4	0xa6	0xa7

Table 1. Device addresses

It is not possible to read from the DSP. The DSP is a write only device.
EEPROM page 3 and 4 are protected by a password!

The DSP settings are directly mapped on EEPROM page 1.

6.2 I^2C Address

The camera has an extra I^2C address, which can be programmed so that more than one camera can be connected to I^2C bus. **The camera default has address 0x70.** If a user forgets the new address, address 0x70 can always be used.

The new I^2C address is stored in the EEPROM page 2 Address 0x90 (hex)
XX is free to choose. With this method a user can have 255 (0x70 is already used as default) different I^2C addresses for the camera.

To change this address one should write: device 0xa2; address 0x90: value 0xXX.
One can read the device 0xa3 value.

6.3 Register Settings

Address	Name	Bit	Function
02	NI	[6]	0: Interlace 1: Non-interlace
	MODE_OUT_SIG	[5:3]	Do not change!
	START_EE	[2]	Shutter speed at power-on, 0: minimum 1: maximum
	AGC_FIX	[1]	AGC control, 0: Auto 1: Fixed
04	SW_CTRL	[7:0]	MIR(MSB),EEMDS,EEMD1,EEMD2,EEMD3,BLC,WB2,WB1(LSB) For explanation see shutter-speed table 1 and white balance table
05	MIN_SH_SEL	[7]	Select minimum shutter speed 0: 1/60(1/50) 1: 1/100(1/120)
	MAX_SH	[6:0]	Maximum shutter speed setting (Set SW CTRL register (address0x04) to EEMDS =1 , EEMD1 =1 , EEMD2=1,EEMD3=0) Contact Videology for details.
06	REF_IRIS1	[7:0]	Reference of exposure: set point of camera
09	REF_IRIS2	[7:0]	Exposure reference in condition against light (When BLC=H)
1B	MAX_AGC	[7:0]	Upper limitation of AGC control.
1C	REF_AGC	[7:0]	Lower limitation of AGC control (initial value of AGC at power-on).
1D	S_38M_GA	[7:0]	Fixed gain [bit7:0 (LSB)]
1E	S_38M_GA_U	[3]	Fixed gain [bit 8(MSB)]
24	C_GAM	[5:3]	Select characteristics of color gamma. Color gamma default bit [5:3] = 010 Color gamma 1 then bit [5:3] = 111
42	WBR1	[7:0]	WB mode 1 (indoor 3200K) White balance Red gain
43	WBB1	[7:0]	WB mode 1 (indoor 3200K) White balance Blue gain
44	WBR2	[7:0]	WB mode 2 (4500K) White balance Red
45	WBR2	[7:0]	WB mode 2 (4500K) White balance Blue gain
46	WBR3	[7:0]	WB mode 3 (outdoor 6400K) White balance Red gain
47	WBB3	[7:0]	WB mode 3 (outdoor 6400K) White balance Blue gain

Color saturation settings

Address	Name	Bit	Function
48	REF_GA_R1M	[7:0]	Chrominance gain (green saturation) of R-Y negative direction when WB1 is fixed or auto control (present WBR factor = WBR1).
49	REF_GA_B1M	[7:0]	Chrominance gain (yellow saturation) of B-Y negative direction when WB1 is fixed or auto control (present WBR factor = WBR1).
4A	REF_GA_R1P	[7:0]	Chrominance gain (red saturation) of R-Y positive direction when WB1 is fixed or auto control (present WBR factor = WBR1).
4B	REF_GA_B1P	[7:0]	Chrominance gain (blue saturation) of B-Y negative direction when WB2 is fixed or auto control (present WBR factor = WBR1).
4C	REF_GA_R2M	[7:0]	Chrominance gain (green saturation) of R-Y negative direction when WB2 is fixed or auto control (present WBR factor = WBR2).
4D	REF_GA_B2M	[7:0]	Chrominance gain (yellow saturation) of B-Y negative direction when WB2 is fixed or auto control (present WBR factor = WBR2).
4E	REF_GA_R2P	[7:0]	Chrominance gain (red saturation) of R-Y positive direction when WB2 is fixed or auto control (present WBR factor = WBR2).
4F	REF_GA_B2P	[7:0]	Chrominance gain (blue saturation) of B-Y negative direction when WB2 is fixed or auto control (present WBR factor = WBR2).
50	REF_GA_R3M	[7:0]	Chrominance gain (green saturation) of R-Y negative direction when WB3 is fixed or auto control (present WBR factor = WBR3).
51	REF_GA_B3M	[7:0]	Chrominance gain (yellow saturation) of B-Y negative direction when WB3 is fixed or auto control (present WBR factor = WBR3).
52	REF_GA_R3P	[7:0]	Chrominance gain (red saturation) of R-Y positive direction when WB3 is fixed or auto control (present WBR factor = WBR3).
53	REF_GA_B3P	[7:0]	Chrominance gain (blue saturation) of B-Y negative direction when WB3 is fixed or auto control (present WBR factor = WBR3).
Address	Name	Bit	Function
7B	Y_GAM	[6:4]	Select characteristics of luminance gamma. Default camera luminantie bit [6:4] = 101 Luminantie gamma = 1, bit [6:4] = 111
	VAPT_OFF	[1]	1: Vertical aperture is OFF
	HAPT_OFF	[0]	1: Horizontal aperture is OFF
7C	APT_HGA	[4-0]	Horizontal aperture gain (a.k.a. contouring)
7E	APT_VGA	[4-0]	Vertical aperture gain
88	SETUP	[5:0]	Adjustment of setup level (complement of 2).
8B	OUTGA	[4:0]	Gain of analog output (1 time at 0x10h).
8C	SYNCLEV	[7:0]	Adjustment of SYNC level.
Note: not all registers are listed! These (not listed) registers are system registers and may not be modified!!!! For more information on special functions please contact Videology.			

7 Specification

	20K13XDIG (NTSC) 21K13XDIG (PAL)	20K14XDIG (NTSC) 21K14XDIG (PAL)	20K15XDIG (NTSC) 21K15XDIG (PAL)
Electrical			
Image device		1/4" IL CCD	
Number of active Picture elements	NTSC: 768 (H) x 492(V) PAL: 752 (H) x 582(V)	NTSC: 510 (H) x 492(V) PAL: 500 (H) x 582(V)	NTSC: 768 (H) x 492(V) PAL: 752 (H) x 582(V)
Horizontal resolution	≥ 520 TVL	≥ 330 TVL	≥ 470 TVL
Sensitivity	< 0.05 Lux (50 IRE) F1.2 3200K, lens transmission 80%, scene reflection 75%	< 0.5 Lux (50 IRE) F1.2 3200K, lens transmission 80%, scene reflection 75%	< 0.9 Lux (50 IRE) F1.2 3200K, lens transmission 80%, scene reflection 75%
Signal to noise ratio		>48 dB (AGC off)	
Gain control		Automatic 36 dB (default) Fixed via software	
AGC detection mode		Average (default)	
White Balance mode		AWB auto white mode Fixed modes selectable via software	
Scan mode		Interlaced (default) Non-interlaced (selectable via software)	
Gamma		0.45 (default) (Selectable via software)	
Back light compensation		Default on (Selectable via software)	
Contour enhance		Default on	
Iris control		Electronic (default) Fixed Shutter speeds selectable via software	
Synchronisation		Internal (X-tal)	
Outputs: Video		1 Vp-p CVBS 75 Ohm 8-bit digital output YUV:422 according CCIR656 c-mos output, 3.3V level. 16-bit digital output CCIR601 c-mos output, 3.3V level.	
Inputs:			
communication		I^2C SDA & SCK 3,3V level.	
Supply Voltage		5V DC ±5% NOT POLARITY PROTECTED.	
Power consumption		< 0.8 Watt	
Mechanical			
Lens mount		CS-mount, optional C-mount with interface ring. Board-lens f=3.7mm or Pinhole or no lens-mount can be supplied	
Image format		1/4"	
Dimensions		22 x 26 x 25mm (LxWxD) without lens (in case of CS-mount)	
Interface		Flex foil connector: 17 pole JST-17FXL-RSM1-S-H-TB. Board to board connector: 30 pole: MOLEX-53916-0304. The mating part is MOLEX-52991-0308	
Interface cables		None	
Environmental			
Ambient operational temperature		-15º to +55º Celsius	
Ambient storage temperature		-25º to +70º Celsius	
Ambient operational humidity		0 to 93%RH	
Ambient storage humidity		Up to 98% RH	
Lifetime		MTBF >150000	
Approbation		TBD	
Packaging		ESD safe package	

8 The Digital Output Format

The 20K14XDIG/20K15XDIG cameras have the following digital output format:

- 8-bit format, i.e. D1 /CCIR656 with the sync code included in the video path
- 16-bit format, i.e. CCIR601 without the sync code in the video data.

*** Please note that for both output formats the clock frequency differs from the CCIR standards.

20K14XDIG (standard resolution): For the 8-bit format, the data rate is 19.091 MHz for NTSC, and 18.916 MHz for PAL, instead of the 27MHz clock frequency specified by the standards. For the 16-bit format the data frequency is 9.545 MHz for NTSC and 9.458 MHz for PAL.

20K15XDIG (high resolution): For the 8-bit format, the data rate is 28.636 MHz for NTSC, and 28.375 MHz for PAL, instead of the 27MHz clock frequency specified by the standards. For the 16-bit format the data frequency is 14.31818 MHz for NTSC and 14.1875 MHz for PAL.

The video data is formatted according to YUV 4:2:2. Accordingly, for each two-pixel pair of Y, there is an associated one U pixel and one V pixel available.

The 16-bit data format is shown below in figure 6:

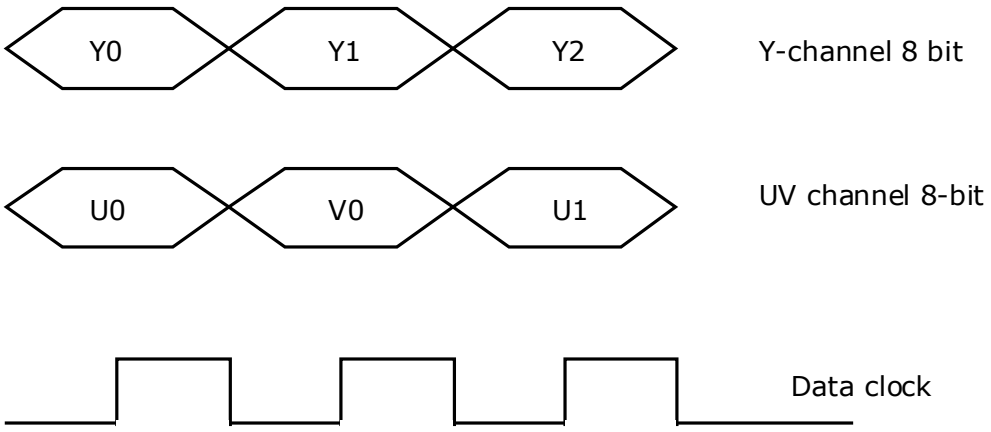


Figure 6. CCIR601 format

The 8-bit data format is shown below in figure 7:

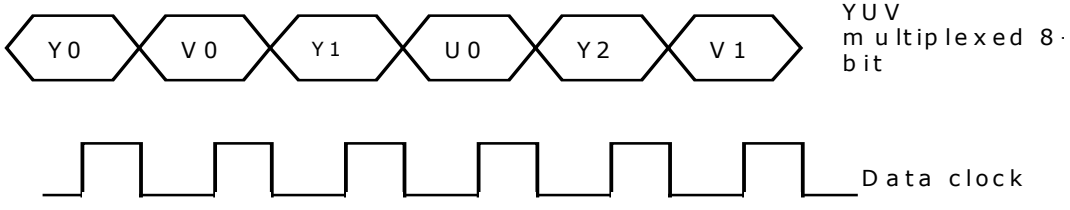


Figure 7. CCIR656 format

A hardware pin can be used to select between the two formats. The camera is in the 8-bit format by default. By pulling the 'DIG_MODE' pin to ground, the camera switches over to the 16-bit format. The 16-bit format is only available on the board-to-board connector on the back of the camera. The 8-bit format is available only via the flex connector at the front of the camera.

20K13XDIG (high resolution): For the 8-bit format, the data rate is 28.636 MHz for EIR, and 28.375 MHz for CCIR, instead of the 27MHz clock frequency specified by the standards.
The video data is formatted according to YUV 4:2:2. Accordingly, for each two-pixel pair of Y, there is an associated one U pixel and one V pixel available.
The camera is Black & White and therefore the UV-levels are set to 0x80 which correspondents to zero.

The 8-bit data format is shown below in figure 8:

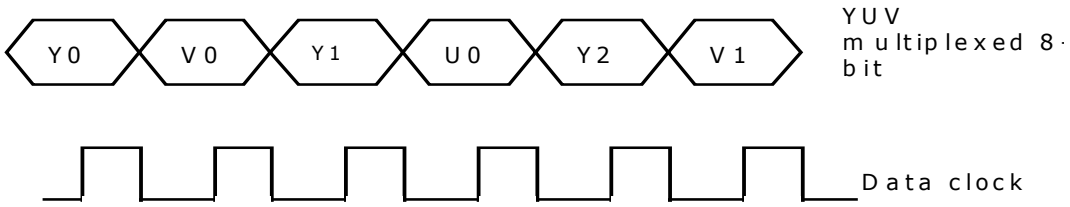


Figure 8. *CCIR656 format*

The 8-bit format is available on the board-to-board connector on the back of the camera and also via the flex connector at the front of the camera.

8.1 Digital Video Compatible ICs

Examples of digital video compatible ICs are listed in the Appendix (section 11).

9 Timing

9.1 Pixel Formatting

In this section, the high frequency pixel timing will be discussed.
Read for 20/21K15XDIG also the 20/21K13XDIG.

9.1.1 8-bit Format

The camera data clock tolerance is 20ppm. A crystal with the same tolerance is used to generate the camera timing. The data clock frequency is:

TV-standard	Nominal frequency	Tolerance +/-
NTSC	28636360 Hz	1431 Hz
PAL	28375000 Hz	1419 Hz

The timing is shown in figure 8 below:

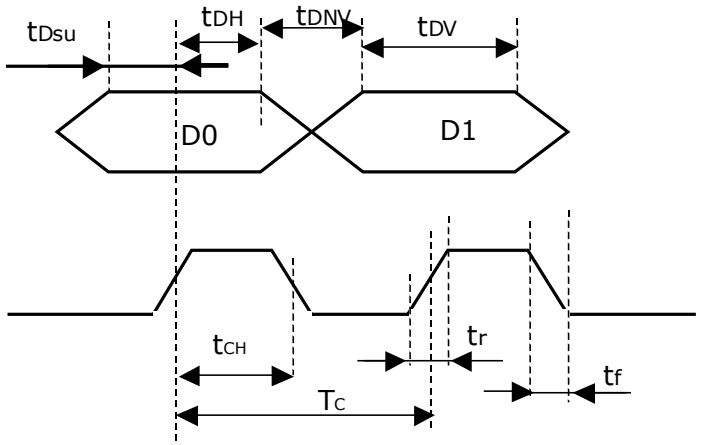


Figure 9. Pixel Timing

Item	description	NTSC:20K14X		PAL: 21K14X		NTSC: 20K15X		PAL: 21K15X	
		min(ns)	max(ns)	min(ns)	max(ns)	min(ns)	max(ns)	min(ns)	max(ns)
T_C	Clock period	52.378	52.386	52.860	52.866	34.918	34.922	35.240	35.244
t_{CH}	Clock high time	22	30	22	30	15	19	15	19
t_r	Rise time		5		5		5		5
t_f	Fall time		5		5		5		5
t_{Dsu}	Data setup	15		15		10		10	
t_{DH}	Data Hold	10		10		7		7	
t_{DNV}	Data not valid		20		20		14		14
t_{DV}	Data valid	30		30		21		21	

The timing relationship between HREF, pixel clock and synchronization data is shown in figure 9:

t_{BL}= NTSC/EIA: 10.9uS (208 clock cycles 20K14X, 312 clock cycles 20K15X), PAL/CCIR: 11.84uS (224 clock cycles 20K14X, 336 clock cycles 21K15X)

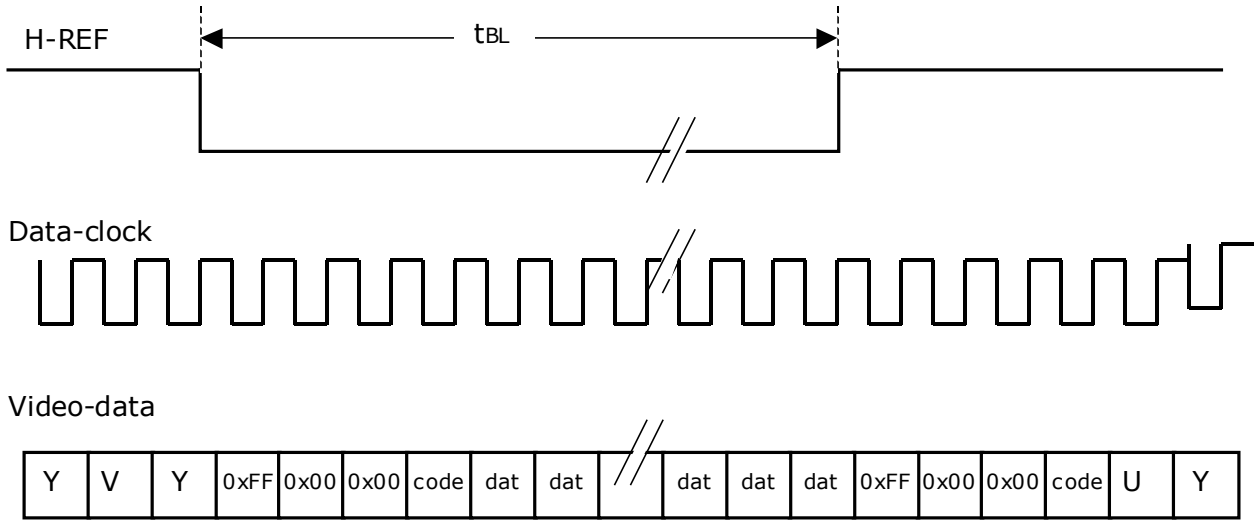


Figure 10. *Pixel sequence during the horizontal blanking (8-bit format)*

The synchronization code is a combination of 4 bytes. The first three bytes are always the same. The sequence is [0xFF], [0x00] and [0x00]. The values 0xFF and 0x00 will not occur in the normal video. The fourth byte gives the synchronization position. It makes use of 3 different signals: FIELD, VD and HD. The last 4 bits contain a protection code to check if an error occurred during the transfer of this position code's byte.

Function	Bit 7:	Bit 6: FIELD	Bit 5: VD	Bit 4: HD	Bit 3: P3	Bit 2: P2	Bit 1: P1	Bit 0: P0
0	1	0	0	0	0	0	0	0
1	1	0	0	1	1	1	0	1
2	1	0	1	0	1	0	1	1
3	1	0	1	1	0	1	1	0
4	1	1	0	0	0	1	1	1
5	1	1	0	1	1	0	1	0
6	1	1	1	0	1	1	0	0
7	1	1	1	1	0	0	0	1

*** Please note: The **HD** pulse is **Positive** going polarity
The **VD** pulse in **Negative** going polarity

9.1.2 16-bit Format (color only)

The major difference between the 16-bit and 8-bit formats is that the color and luminance signals are not multiplexed to one bus, therefore the data clock is only half the frequency used for the 8-bit format.

The data clock in the 16-bit format is:

TV-standard	Nominal frequency	Tolerance +/-
NTSC	14318180 Hz	715 Hz
PAL	14187500 Hz	710 Hz

The other difference is that the synchronization code is not included in the video information. Therefore the data clock, HREF and VREF must be used for synchronization. VREF and HREF timing is discussed in paragraph 9.2.

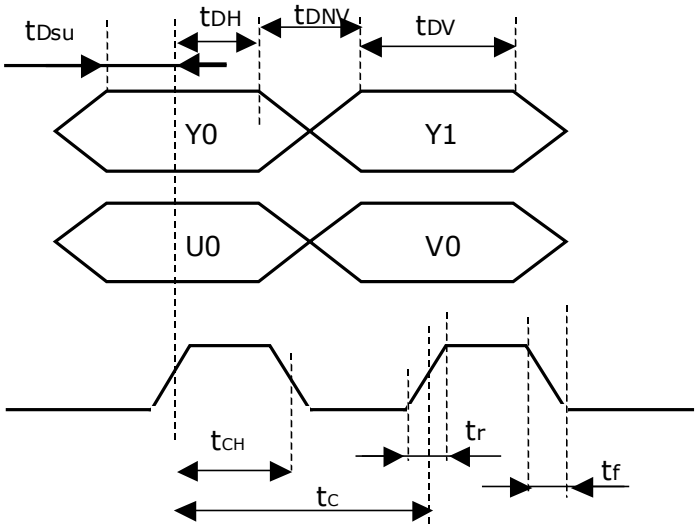


Figure 11. 16-bit timing pixel format

Item	description	NTSC:20K14X		PAL: 21K14X		NTSC: 20K15X		PAL: 21K15X	
		min(ns)	max(ns)	min(ns)	max(ns)	min(ns)	max(ns)	min(ns)	max(ns)
T_C	Clock period	104.76	104.77	105.72	105.73	69.844	69.836	70.48	70.488
t_{CH}	Clock high time	46	58	46	58	30	40	30	40
t_r	Rise time		5		5		5		5
t_f	Fall time		5		5		5		5
t_{Dsu}	Data setup	15		15		10		10	
t_{DH}	Data Hold	10		10		7		7	
t_{DNV}	Data not valid		20		20		14		14
t_{DV}	Data valid	55		55		55		55	

t_{BL}= NTSC: 10.9uS (104 clock cycles 20K14X, 156 clock cycles 20K15X),
PAL: 11.84uS (112 clock cycles 21K14X, 168 clock cycles 21K15X)

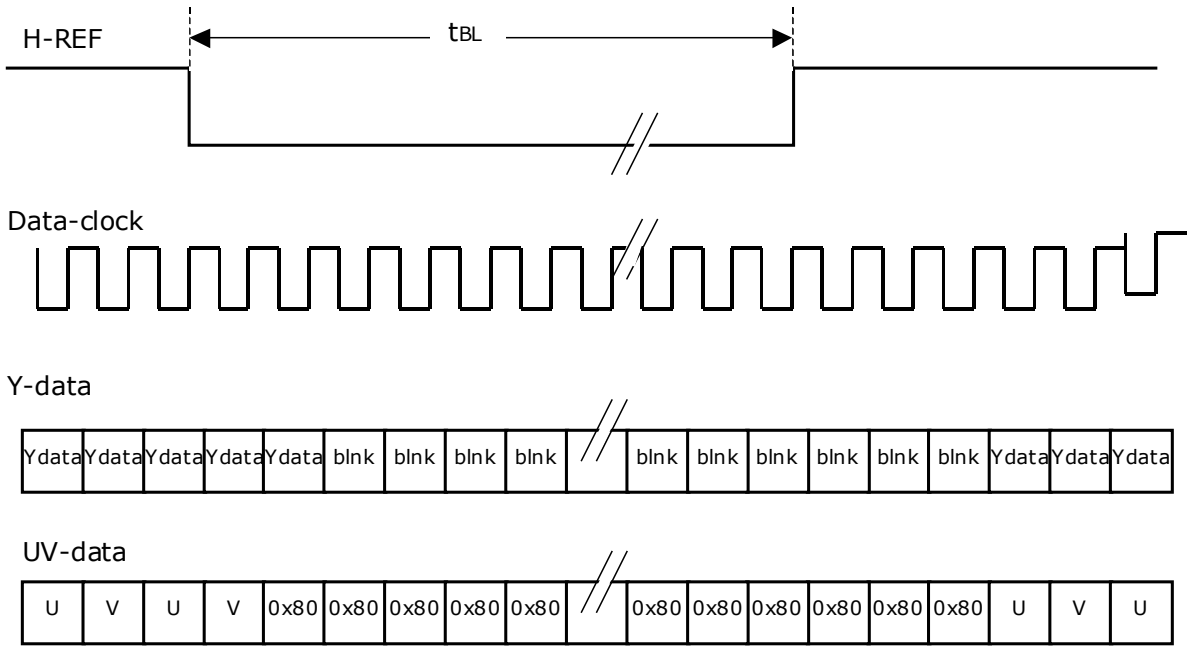


Figure 12. Pixel sequence during the horizontal blanking (16-bit format)

9.2 Horizontal and Vertical Synchronisation

The camera has two independent synchronization signals in the digital format.

- One sync signal is HREF. HREF is a negative oriented pulse, which means that the pulse is low during the horizontal blanking period.
- The other sync signal is VREF. VREF is a positive oriented pulse, which means that it is high during the vertical blanking period. VREF also indicates the vertical period when video is not active.

The relation between HREF and VREF is shown in figure 12 (NTSC) and figure 13 (PAL).

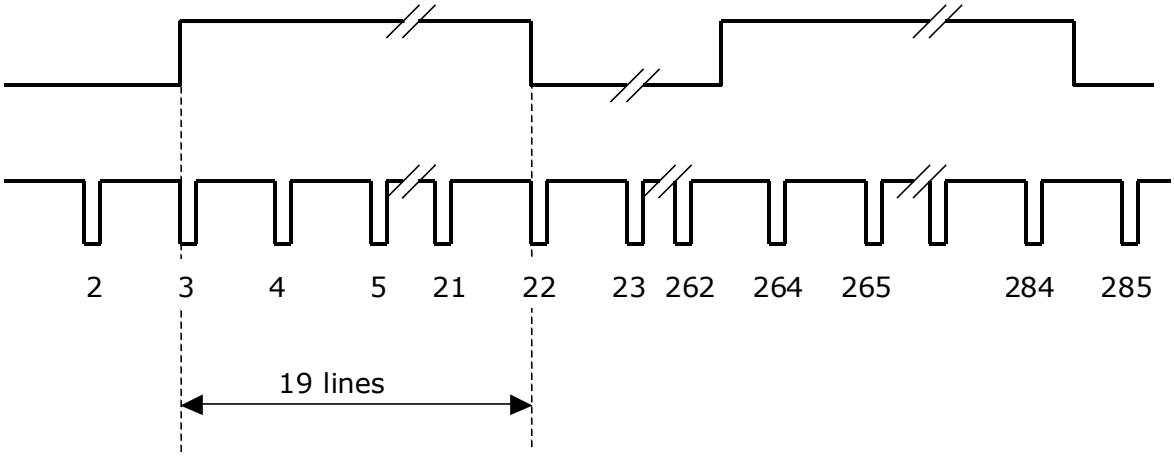


Figure 13. *NTSC vertical timing*

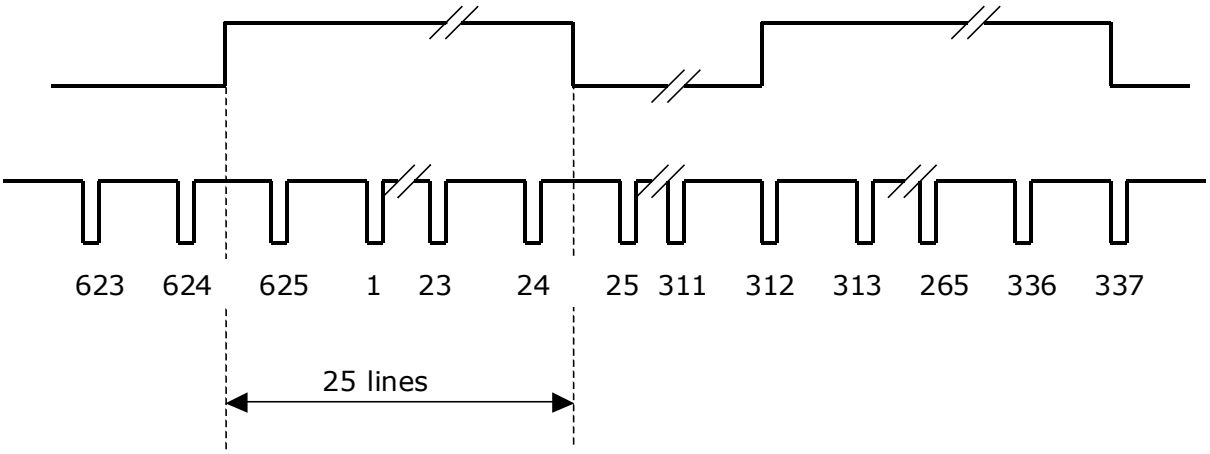


Figure 14. PAL vertical timing

The relationship between HREF and VREF can indicate if the camera is either in FIELD one or FIELD two. A FIELD indication signal can easily be made using a D-flip-flop and connecting VREF to the clock input and HREF to the D–input, as in figure 14.

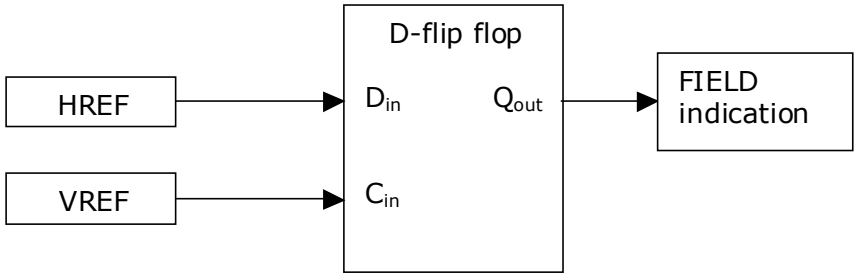


Figure 15. Field detection

For PAL and NTSC the indication level is different, which can be seen in figures 12 and 13.

TV-system	Field 1	Field 2
NTSC	FIELD= low (0)	FIELD= high (1)
PAL	FIELD= high (1)	FIELD= low (0)

10 Connectors

The camera offers two types of connectors to make interconnections as easy as possible.

- On the backside of the board there is a board-to-board connector.
- On the front side (CCD side) there is a flex foil connector for those applications that require a longer distance between the camera and application.

10.1 Board-to-Board Connector J1

This connector is by Molex with type number: MOLEX-53916-0304. The mating part is MOLEX-52991-0308, and must be used on the application side.

The connector is 30-pole and the pin out can be found in the table below:

10.1.1 20/21K14XDIG 20/21K15XDIG

Pin number	Function	Pin number	Function
1	GROUND	16	(opt. UV6 in CCIR601 format)
2	GROUND	17	YUV7 CCIR656 (Y7 in CCIR601 format)
3	YUV0 CCIR656 (Y0 in CCIR601 format)	18	(opt. UV7 in CCIR601 format)
4	(opt. UV0 in CCIR601 format)	19	Data Clock
5	YUV1 CCIR656 (Y1 in CCIR601 format)	20	Clock1
6	(opt. UV1 in CCIR601format)	21	iris out
7	YUV2 CCIR656 (Y2 in CCIR601 format)	22	GROUND
8	(opt. UV2 in CCIR601 format)	23	HREF
9	YUV3 CCIR656 (Y3 in CCIR601 format)	24	VREF
10	(opt. UV3 in CCIR601 format)	25	Cam_Ready (1)
11	YUV4 CCIR656 (or Y4 in CCIR601 format)	26	Dig_Mode (2)
12	(opt. UV4 in CCIR601 format)	27	I^2C data
13	YUV5 CCIR656 (Y5 in CCIR601 format)	28	I^2C clock
14	(opt. UV5 in CCIR601 format)	29	CVBS analog out
15	YUV6 CCIR656 (Y6 in CCIR601 format)	30	+5V power supply in

(1) **Cam_Ready -** is a signal that indicates that the camera startup has completed. It can be used as a reset signal if the application requires stable camera signals to start.

(2) **Dig_Mode -** is the signal used to select the 8-bit or 16-bit formats. The camera board has an internal 47K ohm pull-up resistor, so it defaults high to the 8-bit format. When pulled down to ground, the interface runs in the 16-bit format.

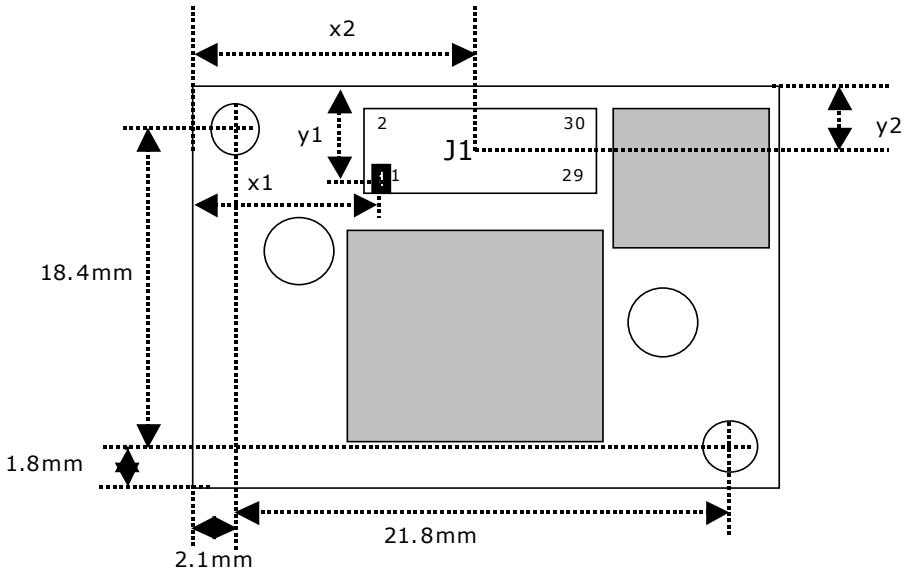


Figure 16. Camera Backside

10.1.2 20/21K13XDIG

Pin number	Function	Pin number	Function
1	GROUND	16	optional
2	GROUND	17	YUV7 CCIR656
3	YUV0 CCIR656	18	optional
4	optional	19	Data Clock
5	YUV1 CCIR656	20	Clock1
6	optional	21	iris out
7	YUV2 CCIR656	22	GROUND
8	optional	23	HREF
9	YUV3 CCIR656	24	VREF
10	optional	25	Cam_Ready (1)
11	YUV4 CCIR656	26	Dig_Mode (2)
12	optional	27	I^2C data
13	YUV5 CCIR656	28	I^2C clock
14	optional	29	CVBS analog out
15	YUV6 CCIR656 optional	30	+5V power supply in

1. **Cam_Ready -** is a signal that indicates that the camera startup has completed. It can be used as a reset signal if the application requires stable camera signals to start.

2. **Dig_Mode** - Optional.

Note: UV-level is always set to 0x80 which refers to zero for UV.

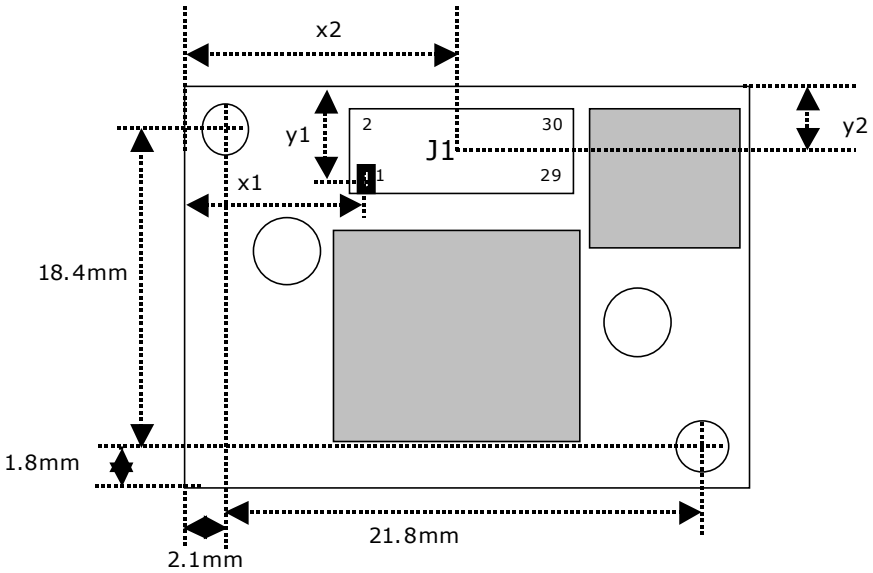


Figure 17. Camera Backside

10.2 Flex Foil Connector J2

This connector is by JST with type number: JST-17FXL-RSM1-S-H-TB. The mating part can be the same type, and should be connected by a flex foil with a pitch of 0.3 mm.

Position of connector J1:
Pin 1 connection J1: x1 = 8.65mm; y1 = 4.75mm
Center position J1: x2 = 12.2mm; y2 = 3.0mm

The connector is 17-pole and the pin out can be found in the table below:

10.2.1 20/21K13XDIG (B&W) 20/21K14XDIG (color) 20/21K15XDIG (color)

Pin number	Function	Pin number	Function
1	I^2C data	10	YUV (4)
2	I^2C clock	11	YUV (5)
3	GROUND	12	YUV (6)
4	Data Clock	13	YUV (7)
5	+5 V power in	14	Clock1
6	YUV (0)	15	GROUND
7	YUV (1)	16	HREF
8	YUV (2)	17	VREF
9	YUV (3)		

Note: UV-level for the 20/21K13XDIG is always set to 0x80 which refers to zero for UV.

The connector position J2 can be found in figure 16:

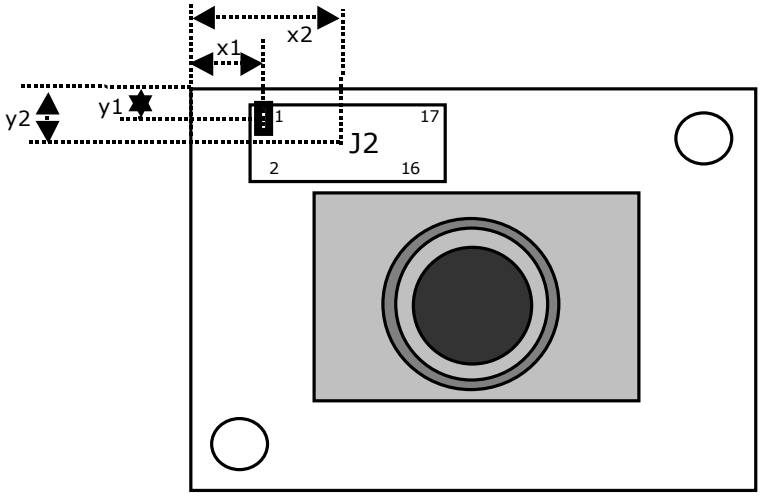


Figure 18. Camera Front-side

Position of connector J2:
Pin 1 connection J2: x1 = 5.8mm; y1 = 0.8mm
Center position J2: x2 = 8.2mm; y2 = 2.8mm

11 Appendix

Digital Video Compatible Ics									
Chip	**Company**	**Description**	**CCIR656 / 8 bit digital input**	**CCIR 601 / 16 bit digital input**	**USB 2.0 output**	**Frames per second / resolution**	**Analog Video input**	**Compression**	**Video output**
EM2800	Empia	video controller USB2.0	Yes	Yes	Yes	30 fps / 720x480	Interlaced, non-interlaced, RGB	Proprietary	
SAA7120	Philips	Digital Video Encoder	Yes					MPEG	CVBS & YC
TMC2490A	Fairchild	Multistandard Digital Video Encoder	Yes						CVBS & YC
FIE8100	Faraday	32 Bit Embedded CPU Plus Video Encoder - supports constant bit rate & variable bit rate	Yes		Yes	30 fps / 4CIF		MPEG 4	LCD controller & TV encoder
ACEX1K	Altera	CCIR 656 Encoder	Yes						NTSC
ADV7174/9	Analog Devices	PAL / NTSC Video encoder	Yes						CVBS & YC
CX23415	Conexant	USB 2.0 MPEG Codec	Yes		Yes	30 fps / 720x480		MPEG 1 & 2	CVBS, YC & Antenna

12 Contact Information

For technical assistance with this product, please contact the supplier from whom the product was purchased.

For OEM inquiries, contact Videology Imaging Solutions:

North / South America:	**Europe:**
Videology Imaging Solutions Inc. 37M Lark Industrial Parkway Greenville, RI 02828 USA Tel: (401) 949-5332 Fax: (401) 949-5276	Videology Imaging Solutions Europe Neutronenlaan 4 NL-5405 NH Uden, Netherlands Tel: +31 (0) 413 256 261 Fax: +31 (0) 413 251 712

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